

N-Channel MOSFET MEM8205F

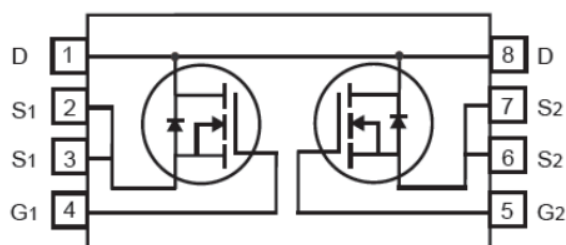
General Description

MEM8205FG Dual N-channel enhancement mode field-effect transistor, produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications, and low power dissipation.

Features

- 20V/6A
- $R_{DS(ON)} = 20m\Omega @ V_{GS}=4.5V, I_D=6A$
- $R_{DS(ON)} = 21m\Omega @ V_{GS}=3.85V, I_D=5A$
- $R_{DS(ON)} = 26m\Omega @ V_{GS}=2.5V, I_D=4A$
- High Density Cell Design For Ultra Low On-Resistance
- Surface mount package:TSSOP8

Pin Configuration



TSSOP8

Typical Application

- Battery management
- Power management
- Portable equipment
- Low power DC to DC converter.
- Load switch
- LCD adapter

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	20V	V
Gate-Source Voltage	V_{GSS}	± 12	V
Drain Current	I_D	6	A
Pulsed Drain Current ^{1,2}	I_{DM}	20	A
Total Power Dissipation	P_d	SOT23-6	1.25
		TSSOP8	1.5
operating junction temperature	T_j	150	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65/150	$^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Ambient ³	$R_{\theta JA}$	100	$^{\circ}C/W$

Electrical Characteristics

MEM8205FG

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	21.5		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.66	1	V
Gate-Body Leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=12V$			100	nA
		$V_{DS}=0V, V_{GS}=-12V$			-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V$		2.5	1000	nA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=6A$		20	24	m Ω
		$V_{GS}=3.85V, I_D=5A$		21	25	m Ω
		$V_{GS}=2.5V, I_D=4A$		26	35	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=4.5A$		10		S
Drain-Source Diode Forward Current	I_S				1.7	A
Source-drain (diode forward) voltage	V_{SD}	$V_{GS}=0V, I_S=1.25A$		0.8	1.0	V
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=8V, V_{GS}=0V, f=1MHz$		600		pF
Output Capacitance	C_{oss}			330		
Reverse Transfer Capacitance	C_{rss}			140		
Switching Characteristics						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=10\Omega, I_D=1A, V_{GEN}=4.5V, R_g=6\Omega$		8	20	ns
Rise Time	t_r			10	25	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall-Time	t_f			30	60	
Total Gate Charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V, I_D=6A$		10	15	nC
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			2.9		

- 1、Pulse width limited by Max. junction temperature.
- 2、Pulse width <300us , duty cycle <2%.
- 3、Surface Mounted on FR4 Board, t < 10 sec.

Typical Performance Characteristics

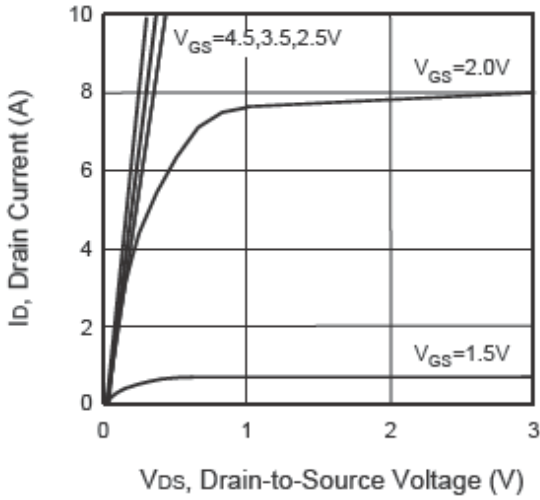


Figure 1. Output Characteristics

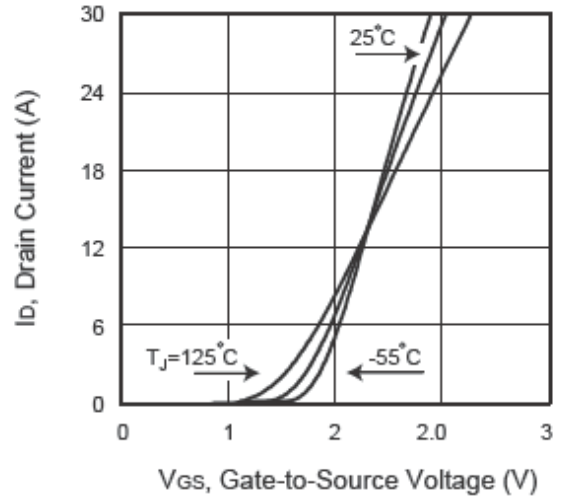


Figure 2. Transfer Characteristics

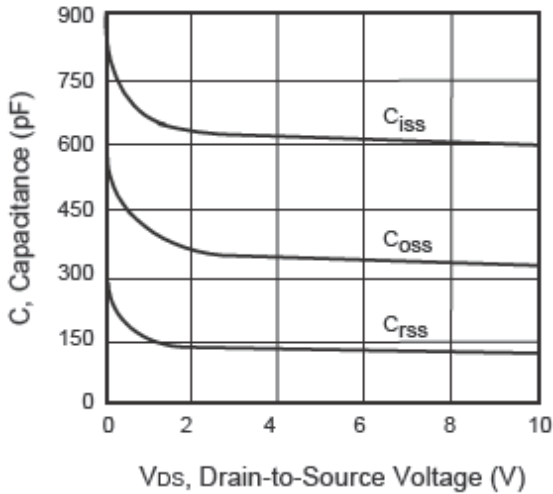


Figure 3. Capacitance

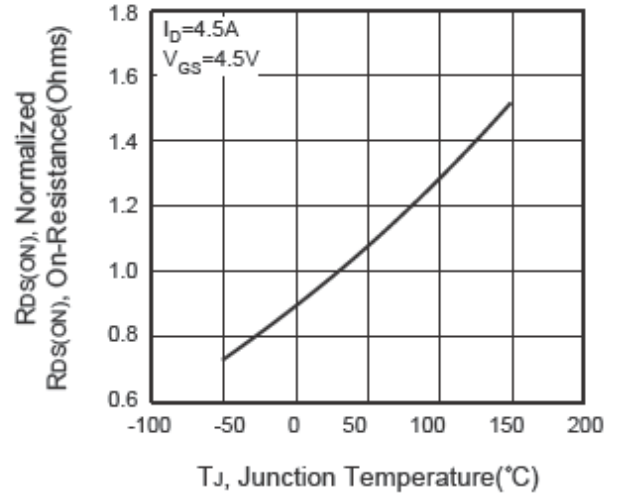


Figure 4. On-Resistance Variation with Temperature

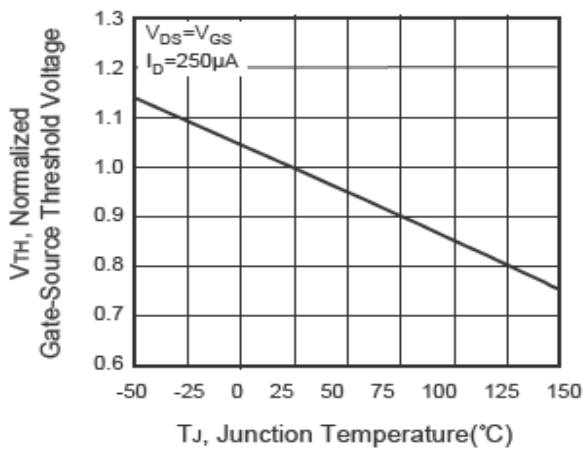


Figure 5. Gate Threshold Variation with Temperature

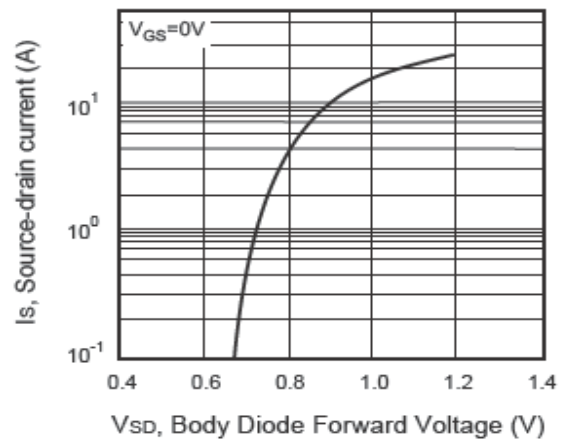


Figure 6. Body Diode Forward Voltage Variation with Source Current

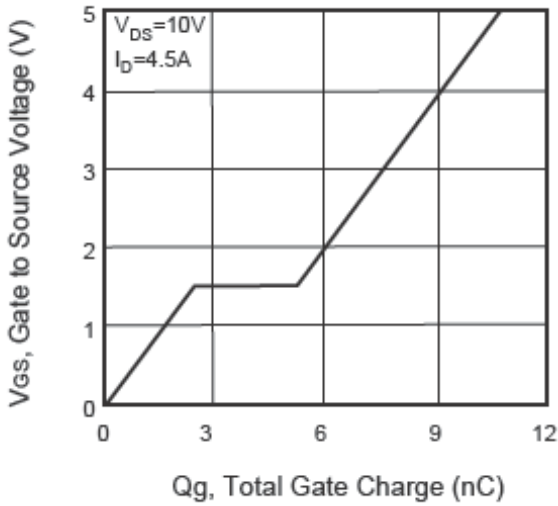


Figure 7. Gate Charge

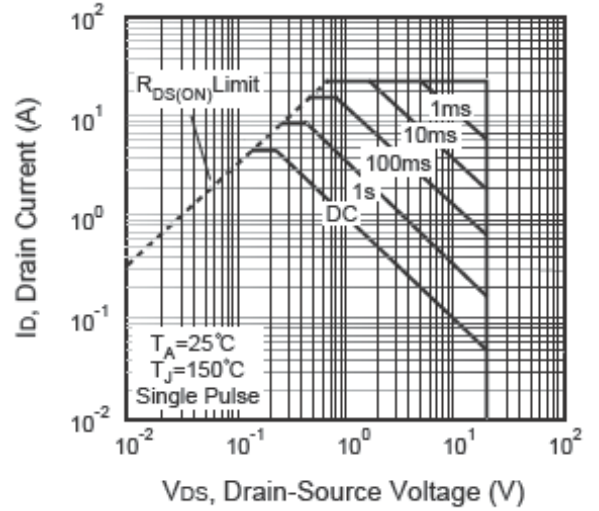


Figure 8. Maximum Safe Operating Area

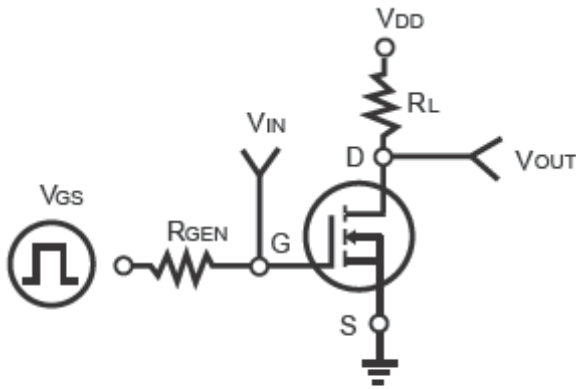


Figure 9. Switching Test Circuit

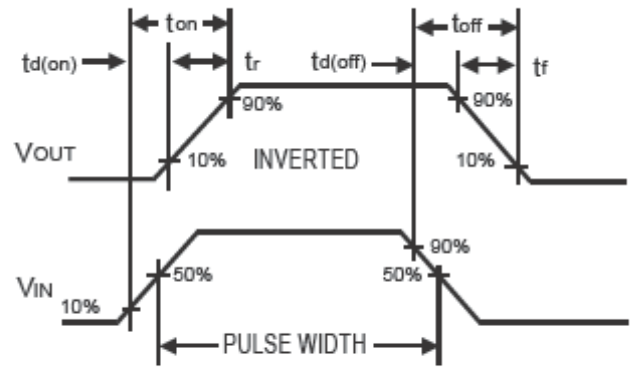


Figure 10. Switching Waveforms

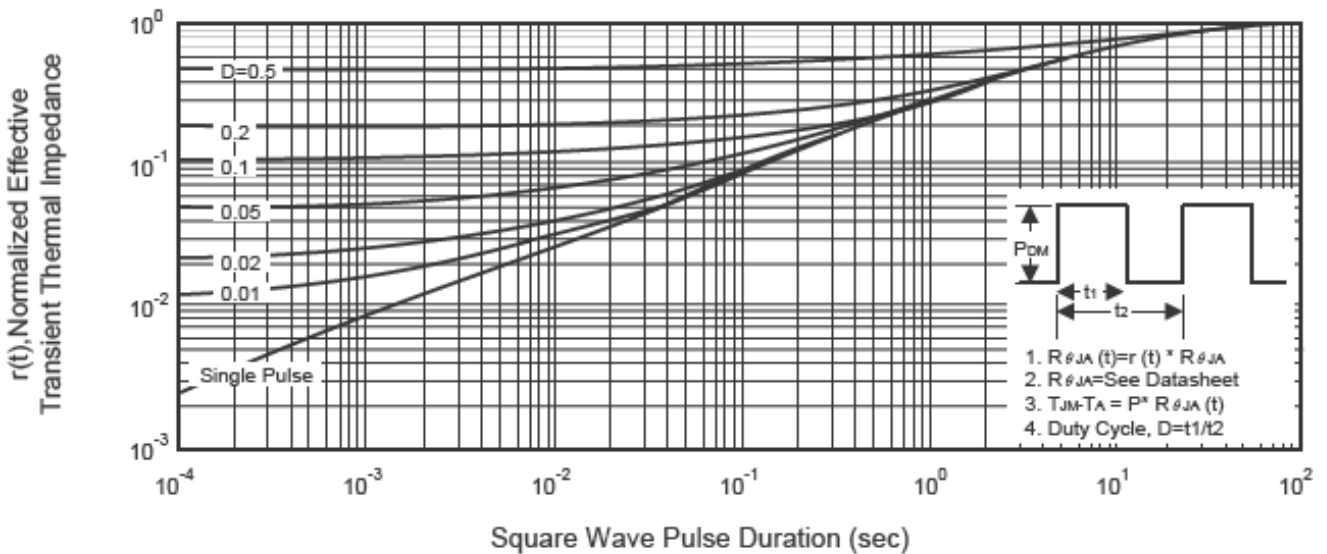
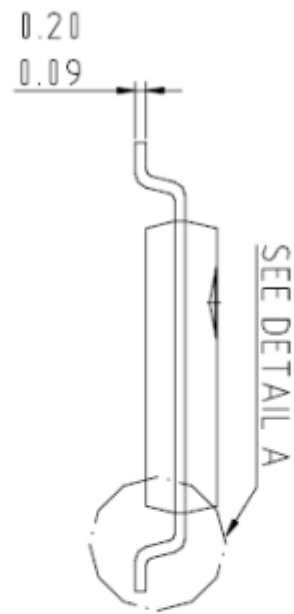
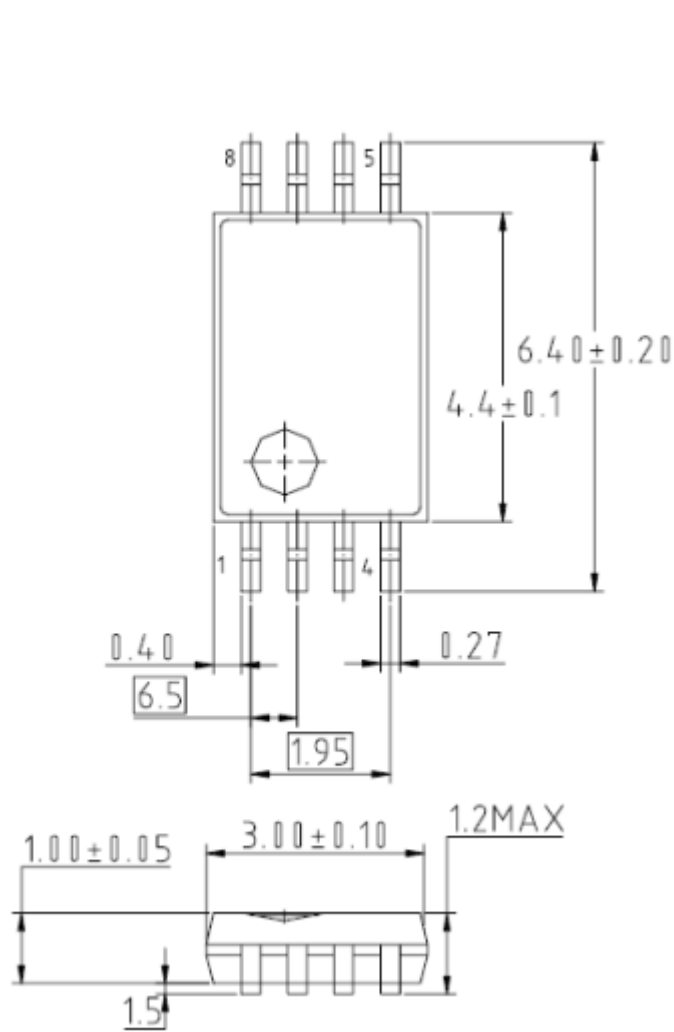


Figure 11. Normalized Thermal Transient Impedance Curve

Package Information



TSSOP8
Unit:mm

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