Voltage Detector with Delay Time Adjustable ME2815

General Description

The ME2815 series is highly precise, low power consumption voltage detector ，The device includes the built-in delay circuit. A release delay time can be set freely by connecting an external delay capacitor to the Cd pin. Both CMOS and N-channel open drain output configurations are available. The ME2815 series is design for CMOS output configurations.

Features

- High Accuracy ： ±1%
- Low Power Consumption ：0.5uA
- Detect Voltage Range：
  1.0V~5.0V (0.1V increments)
- Operating Voltage Range：0.7V~6.0V
- Detect Voltage Temperature Characteristics：
  ±100ppm/℃ TYP
- Output Configurations：CMOS
- Built-In Delay Circuit ：Delay Time Adjustable
- Operating Ambient Temperature ：-40℃~ +85 ℃

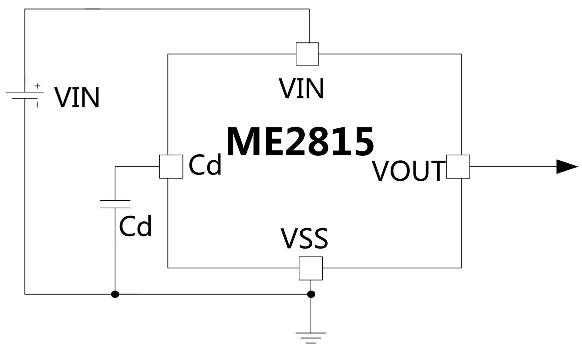
Applications

- Microprocessor reset circuitry
- Charge voltage monitors
- Memory battery back-up switch circuits
- Power failure detection circuits

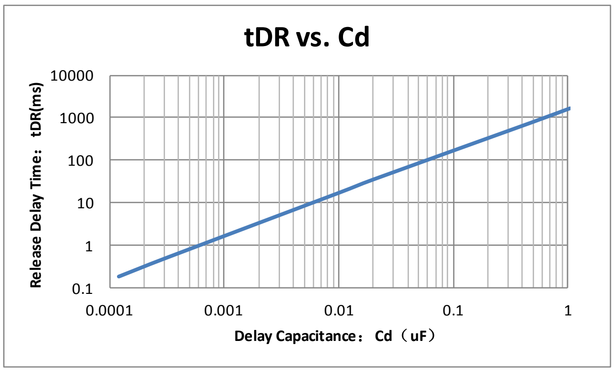
Packages

- 5-pin SOT23-5

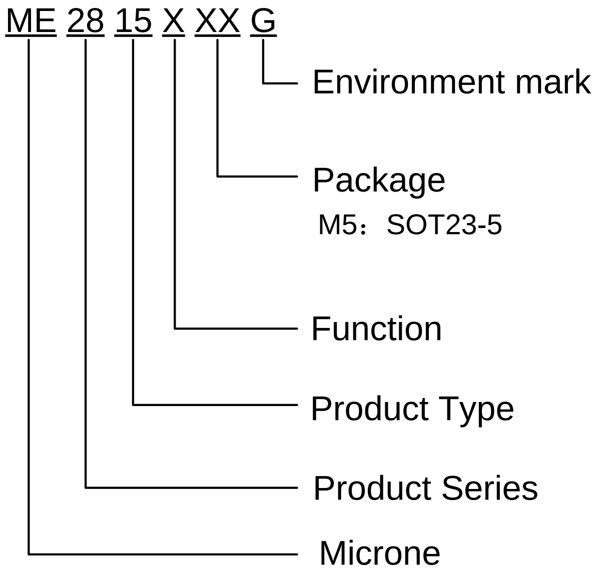
Typical Application Circuit



Release Delay Time vs. Delay Capacitance



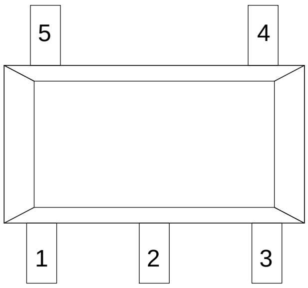
Selection Guide



product series	product description
ME2815A33M5G	Package：SOT23-5

NOTE：If you need other voltage and package, please contact our sales staff。

Pin Configuration

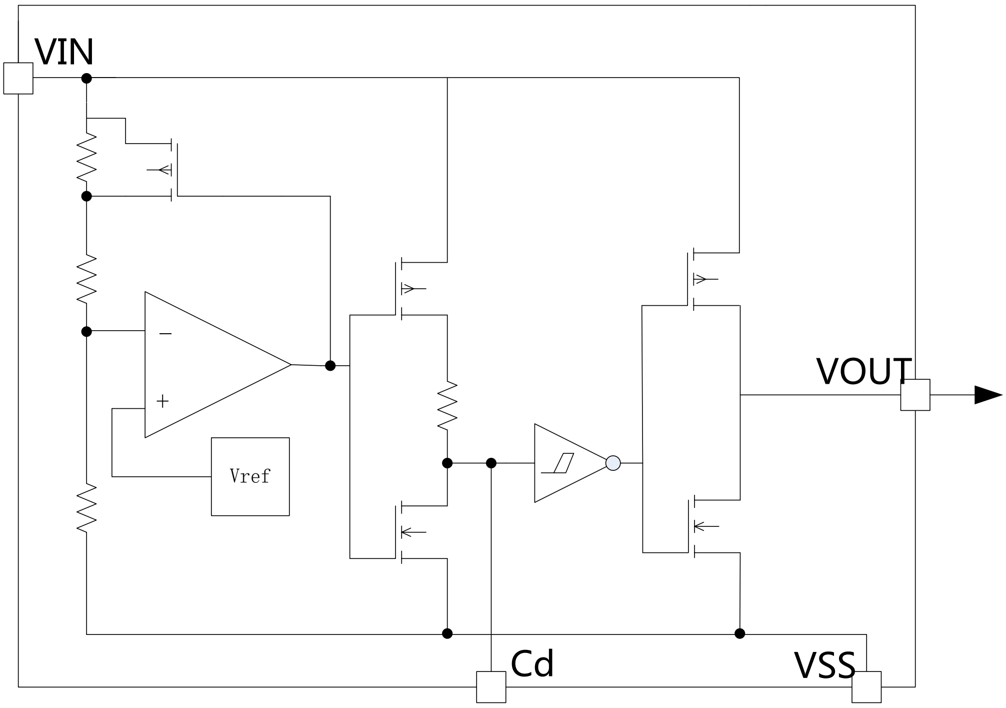


SOT23-5

Pin Assignment

Pin Number	Pin Name	Functions
SOT23-5		
1	VIN	Input
2	NC	No Connection
3	VSS	Ground
4	Cd	Delay Capacitance
5	VOUT	Output (Detect ”L”)

Block Diagrams



Absolute Maximum Ratings

PARAMETER		RATINGS	UNITS
Input Voltage VIN		VSS-0.3 ~ 7.0	V
Output Current IOUT		10	mA
Output Voltage VOUT		VSS-0.3～7.0	V
Delay Pin Voltage VCD		VSS-0.3～VIN+0.3	V
Delay Pin Current ICD		5.0	mA
Power Dissipation PD	SOT23-5	300	mW
Operating Ambient Temperature Ta		-40～+85	℃
Storage Temperature Tstg		-55～+150	℃

Note: Exceeding these ratings may damage the device.

Electrical Characteristics (Ta=25℃ unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VIN	VDF(T)=0.8~5.0V (*1)	0.7		6.0	V
Detect Voltage	VDF	VDF(T)=0.8~1.5V	VDF(T)*0.98	VDF(T)	VDF(T)*1.02	V
		VDF(T)=1.6~5.0V	VDF(T)*0.99	VDF(T)	VDF(T)*1.01	V
Hysteresis Width	VHYS	VIN=1.0~6.0V	VDF ×0.02	VDF ×0.05	VDF ×0.08	V
Supply Current	ISS			0.5	1.2	μA
Output Current	IOUT1	VIN=0.7V DS=0.5V(Nch)	0.01	0.36		mA
		VIN=1.0V(*2) DS=0.5V(Nch)	0.1	0.7		
		VIN=2.0V(*3) DS=0.5V(Nch)	0.8	1.6		
		VIN=3.0V(*4) DS=0.5V(Nch)	1.2	2.0		
		VIN=4.0V(*5) DS=0.5V(Nch)	1.6	2.3		
	IOUT2	VIN=5.5V DS=0.5V(Pch)	3	5		mA
Delay Resistance (*6)	Rdelay	VIN=6.0V, Cd=0V	1.6	2.0	2.4	MΩ
Temperature Characteristics	△VDF/ △Ta*VDF	Ta=-40℃~150℃		100		ppm
Delay Pin Sink Current	ICD	Cd=0.5V, VIN=0.7V	8	60		μA
Delay Capacitance Pin Threshold Voltage	VTCD	VIN=1.0V	0.4	0.5	0.6	V
		VIN=6.0V	2.9	3.0	3.1	

Notes:

*1 VDF(T) Setting Detect Voltage

*2: VDF(T)>1V

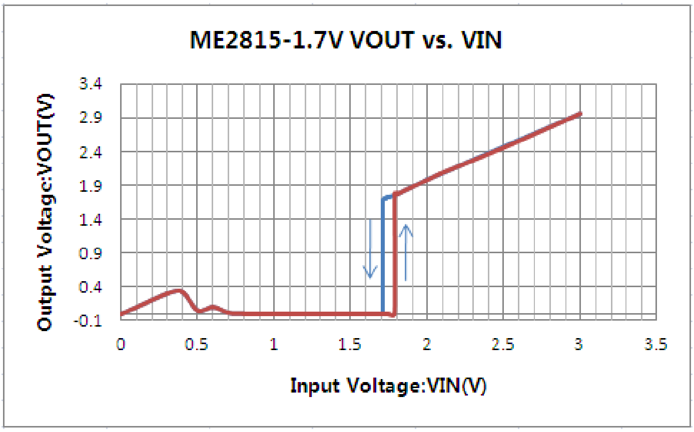
*3: VDF(T)>2V

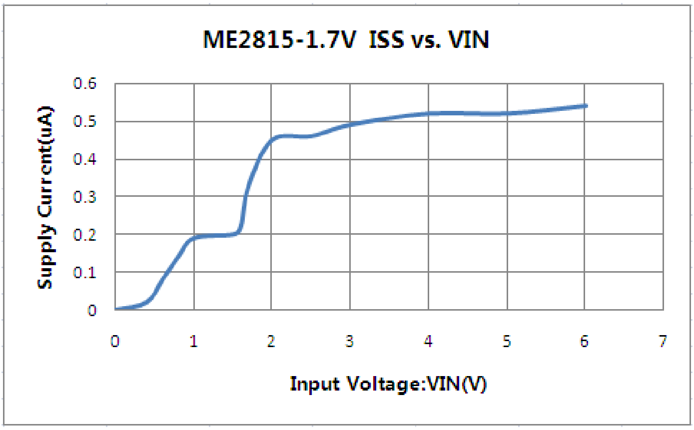
*4: VDF(T)>3V

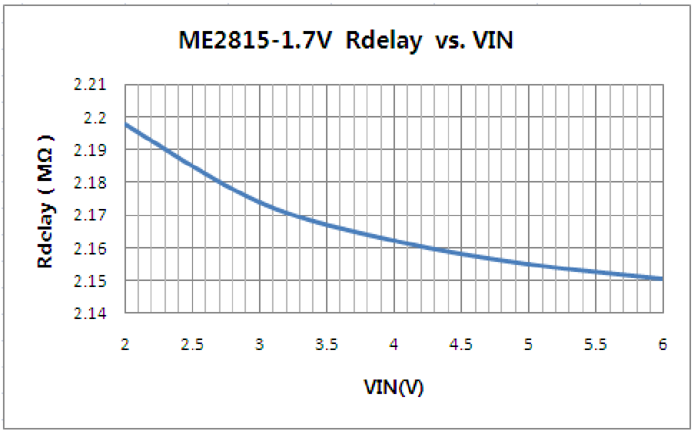
*5: VDF(T)>4V

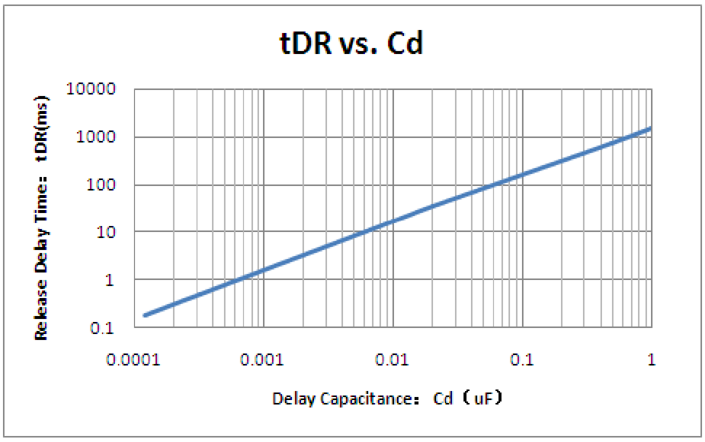
*6: Calculated from the voltage value and the current value of both ends of the resistor.

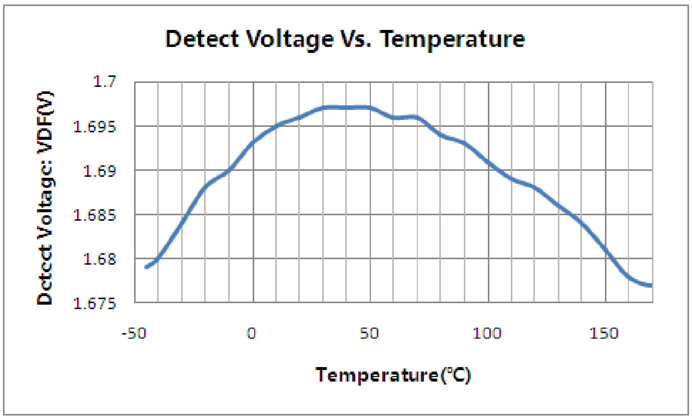
Typical Performance Characteristics

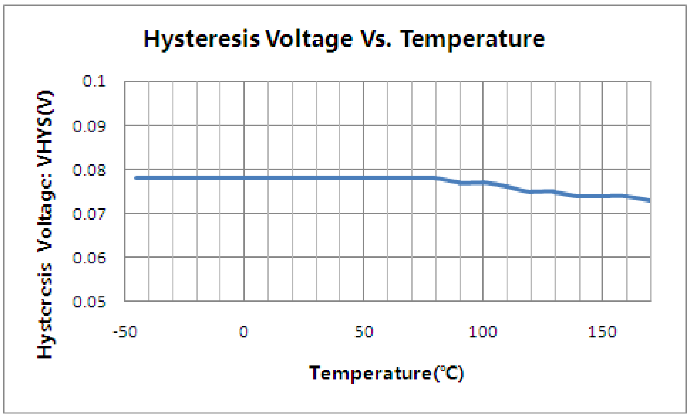












Operational Explanation：

A typical circuit example is shown in Figure 1, and the timing chart of Figure 1 is shown in Figure 2.

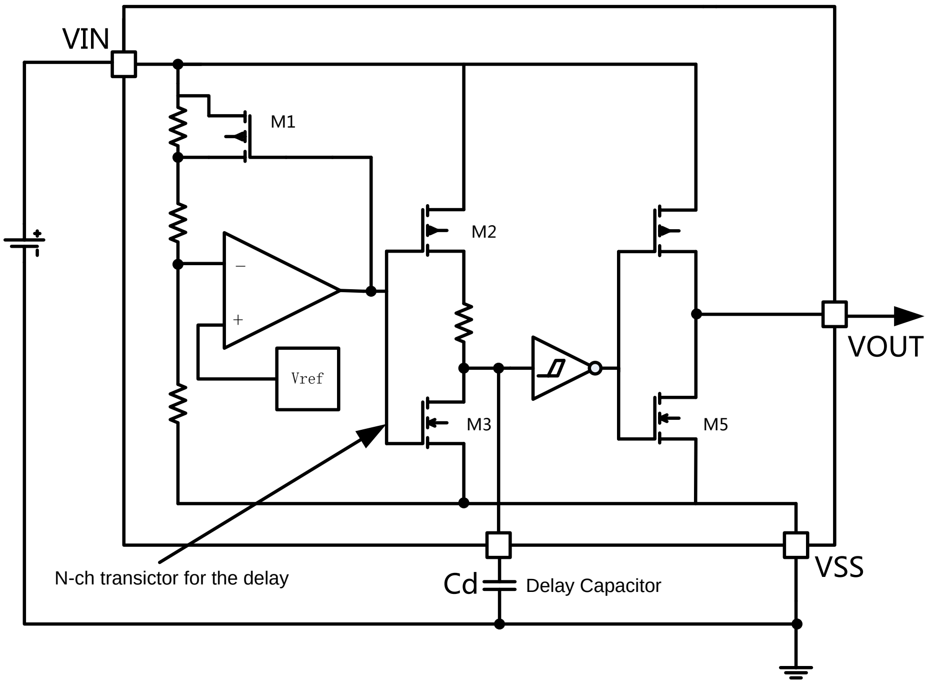


Figure 1: Typical application circuit example

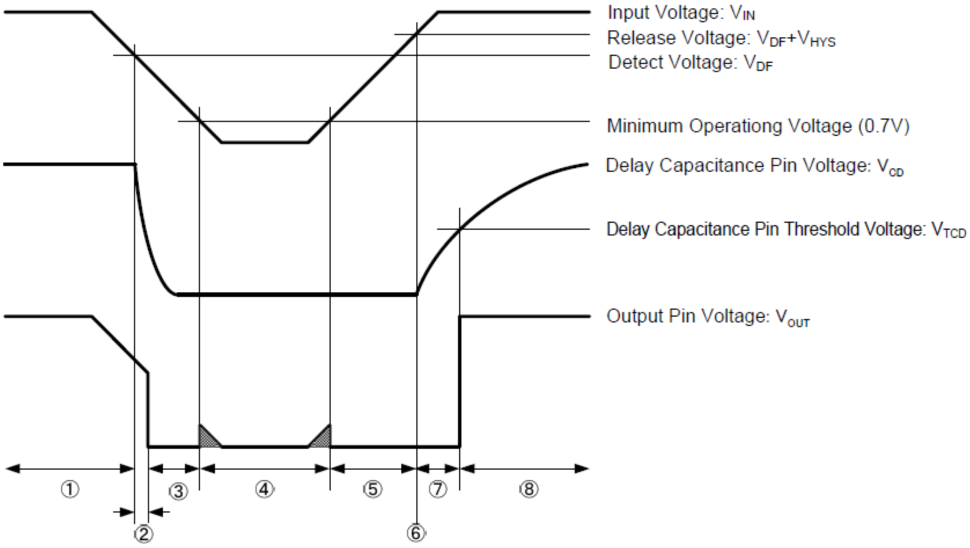


Figure 2: The timing chart of Figure 1

1) As an early state, the input voltage pin is applied sufficiently high voltage to the release voltage and the delay capacitance (Cd) is charged to the input pin voltage. While the input pin voltage (VIN) starts dropping to reach the detect voltage (VDF) (VIN > VDF), the output voltage (VOUT) keeps the “High” level (=VIN).
2) When the input pin voltage keeps dropping and becomes equal to the detect voltage (VIN = VDF), an N-ch transistor for the delay capacitance discharge is turned ON, and starts to discharge the delay capacitance.

For the internal circuit, which uses the delay capacitance pin as power input, the reference voltage operates as a comparator of VIN, and the output voltage changes into the “Low” level (≦VIN×0.1). The detect delay time (tDF) is defined as time which ranges from VIN =VDF to the VOUT of “Low” level (especially, when the Cd pin is not connected: tDF0).

3) While the input pin voltage keeps below the detect voltage, and 0.7V or more, the delay capacitance is discharged to the ground voltage (=VSS) level. Then, the output voltage (VOUT) maintains the “Low” level.

4) While the input pin voltage drops to less than 0.7V and it increases again to 0.7V or more, the output voltage may not be able to maintain the “Low” level. Such an operation is called “Unspecified Operation”, and voltage which occurs at the output pin voltage is defined as unstable operating voltage (VUNS).

5) While the input pin voltage increases more than 0.7V and it reaches to the release voltage level (VIN＜VDF +VHYS), the output voltage (VOUT) maintains the “Low” level.

6) When the input pin voltage continues to increase more than 0.7V up to the release voltage level (= VDF + VHYS), the N-ch transistor for the delay capacitance discharge will be turned OFF, and the delay capacitance will be started discharging via a delay resistor (RDELAY). The internal circuit, which uses the delay capacitance pin as power input, will operate as a hysteresis comparator (Rise Logic Threshold: VTLH=VTCD, Fall Logic Threshold: VTHL=VSS) while the input pin voltage keeps higher than the detect voltage (VIN > VDF).

7) While the input pin voltage becomes equal to the release voltage or higher and keeps the detect voltage or higher, the delay capacitance (Cd) will be charged up to the input pin voltage. When the delay capacitance pin voltage (VCD) reaches to the delay capacitance pin threshold voltage (VTCD), the output voltage changes into the “High” (=VIN) level. tDR is defined as time which ranges from VIN =VDF+VHYS to the VOUT of “High” level (especially when the Cd pin is not connected: tDR0). tDR can be given by formula (1).

$$tDR = -RDELAY \times Cd \times \ln(1 - VTCD / VIN) + tDR0 \qquad (1)$$

* In = a natural logarithm The release delay time can also be briefly calculated with the formula (2) because the delay resistance is 2.0MΩ(TYP.) and the delay capacitance pin threshold voltage is VIN /2 (TYP.)

$$tDR = RDELAY \times Cd \times 0.69 \qquad (2)$$

* RDELAY is 2.0MΩ(TYP.) As an example, presuming that the delay capacitance is 0.68μF, tDR is :2.0×106×0.68×10-6×0.69=938(ms) * Note that the release delay time may remarkably be short when the delay capacitance is not discharged to the ground (=VSS) level because time described in ③ is short

8) While the input pin voltage is higher than the detect voltage (VIN > VDF), therefore, the output voltage maintains the “High”(=VIN) level.

Release Delay Time Chart

Delay Capacitance [Cd]（uF)	Release Delay Time [Cd]（TYP）（ms）	Release Delay Time [Cd]（MIN.~MAX.）*1（ms）
0.01	13.8	11.0~16.6
0.022	30.4	24.3~36.4
0.047	64.9	51.9~77.8
0.1	138	110~166
0.22	304	243~364
0.47	649	519~778
1.0	1380	1100~1660

* The release delay time values above are calculate by using formula (2).

*1: The release delay time (tDR) is influenced by the release capacitance (Cd).

Notes on Use

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. The input pin voltage drops by the resistance between power supply and the VIN pin, and by through current at operation of the IC. At this time, the operation may be wrong if the input pin voltage falls below the minimum operating voltage range. In CMOS output, for output current, drops in the input pin voltage similarly occur. Oscillation of the circuit may occur if the drops in voltage, which caused by through current at operation of the IC, exceed the hysteresis voltage. Note it especially when you use the IC with the VIN pin connected to a resistor.
3. Note that a rapid and high fluctuation of the input pin voltage may cause a wrong operation.
4. Power supply noise may cause an operational function error. Care must be taken to put an external capacitor between VIN-GND and test on the board carefully.
5. When there is a possibility of which the input pin voltage falls rapidly (e.g.: 6.0V to 0V) at release operation with the delay capacitance pin (Cd) connected to a capacitor, use a schottky barrier diode connected between the VIN pin and the Cd pin as the Figure 3 shown below.

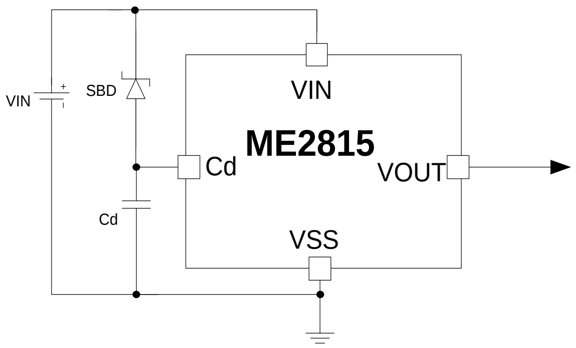
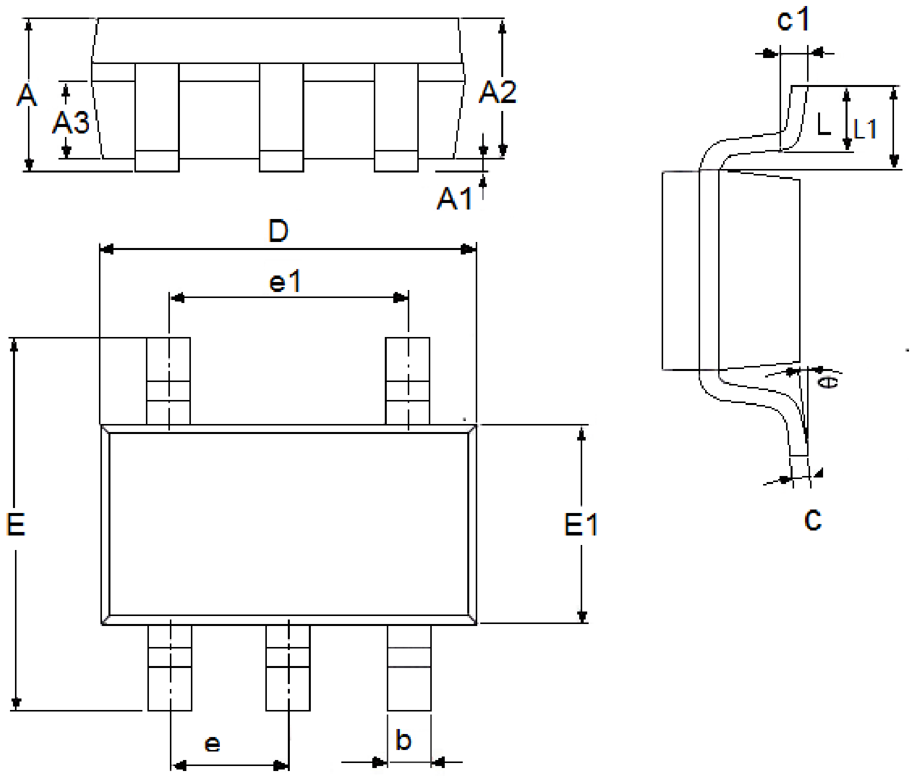


Figure 3: Circuit example with the delay capacitance pin (Cd) connected to a schottky barrier diode

Packaging Information

- SOT23-5



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	1.05	1.45	0.0413	0.0571
A1	0	0.15	0.0000	0.0059
A2	0.9	1.3	0.0354	0.0512
A3	0.6	0.7	0.0236	0.0276
b	0.25	0.5	0.0098	0.0197
c	0.1	0.23	0.0039	0.0091
D	2.82	3.05	0.1110	0.1201
e1	1.9(TYP)		0.0748(TYP)	
E	2.6	3.05	0.1024	0.1201
E1	1.5	1.75	0.0512	0.0689
e	0.95(TYP)		0.0374(TYP)	
L	0.25	0.6	0.0098	0.0236
L1	0.59(TYP)		0.0232(TYP)	
θ	0	8°	0.0000	8°
c1	0.2(TYP)		0.0079(TYP)	

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