



## Description

### JMT P-channel Enhancement Mode Power MOSFET

#### Features

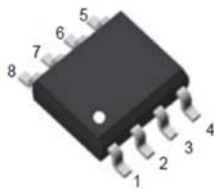
- $V_{DS} = -30V$ ,  $I_D = -10A$   
 $R_{DS(ON)} < 23m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 34m\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

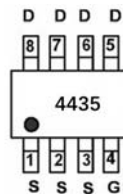
- PWM Applications
- Load Switch
- Power Management



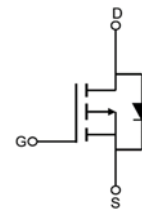
*100% UIS TESTED!*  
*100%  $\Delta V_{ds}$  TESTED!*



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
4435	JMTP4435A	TAPING	SOP-8	13inch	4000	48000

## Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	-10
		$T_C = 100^\circ C$	-7
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	-40	A
$P_D$	Power Dissipation	$T_A = 25^\circ C$	3.7
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	33.8	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> = -250μA	-30	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V,	-	-	-1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.0	-1.5	-2.4	V
R <sub>DSON</sub>	Static Drain-Source on-Resistance <small>note2</small>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	16	23	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5A	-	21	34	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1.0MHz	-	1550	-	pF
C <sub>oss</sub>	Output Capacitance		-	327	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	278	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -15V, I <sub>D</sub> = -9.1A, V <sub>GS</sub> = -10V	-	30	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	5.3	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	7.6	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = -15V, I <sub>D</sub> = -6A, V <sub>GS</sub> =-10V, R <sub>GEN</sub> =2.5Ω	-	14	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	20	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	95	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	65	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	-10	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-40	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = -10A	-	-0.8	-1.2	V

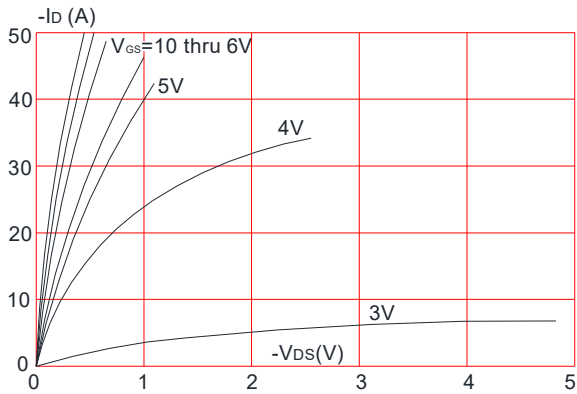
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

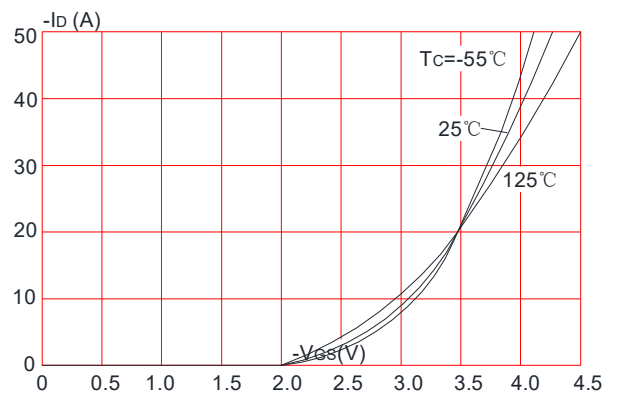


## Typical Performance Characteristics

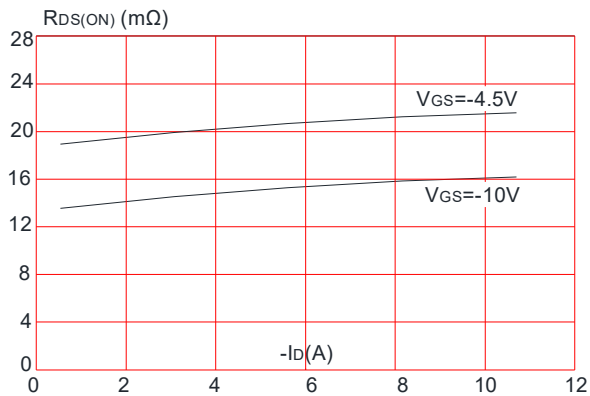
**Figure 1: Output Characteristics**



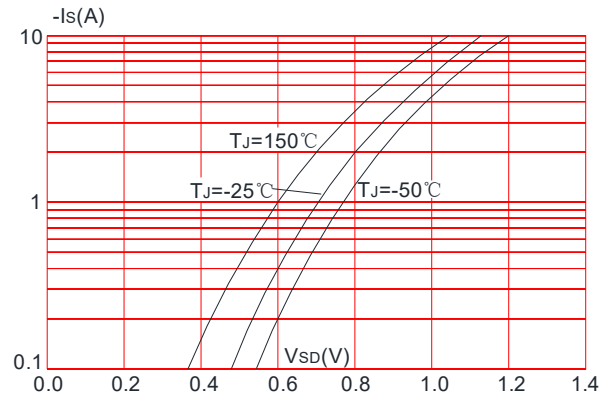
**Figure 2: Typical Transfer Characteristics**



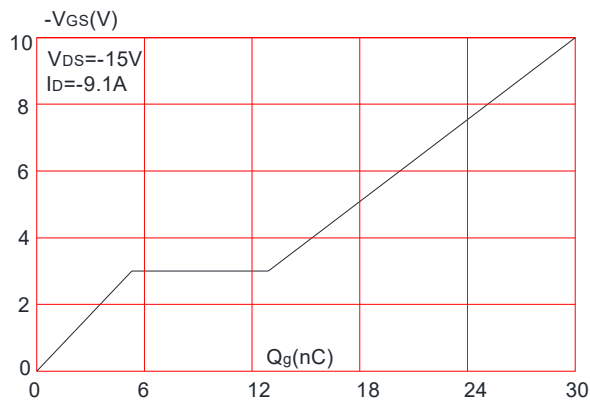
**Figure 3: On-resistance vs. Drain Current**



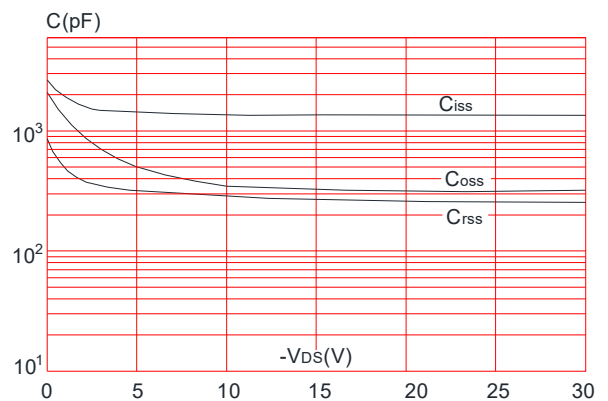
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**

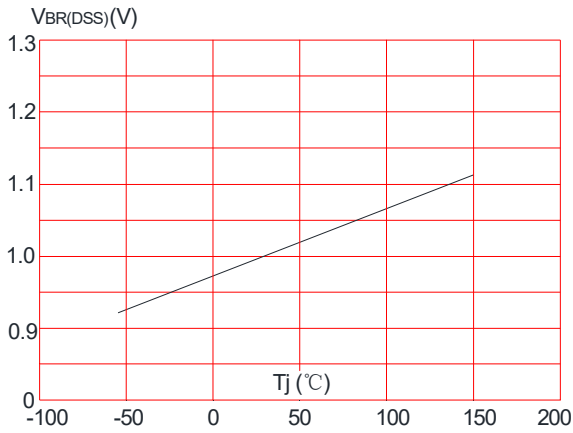


**Figure 6: Capacitance Characteristics**

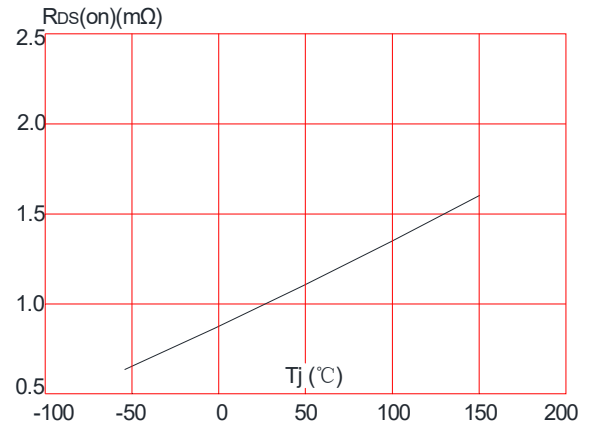




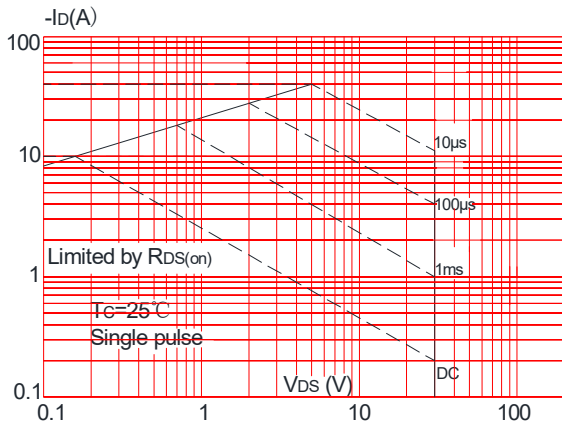
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



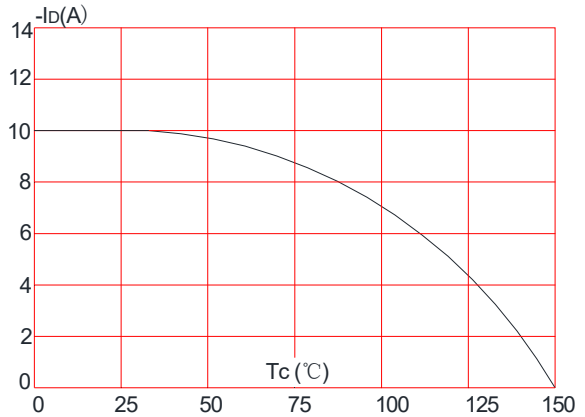
**Figure 8:** Normalized on Resistance vs. Junction Temperature



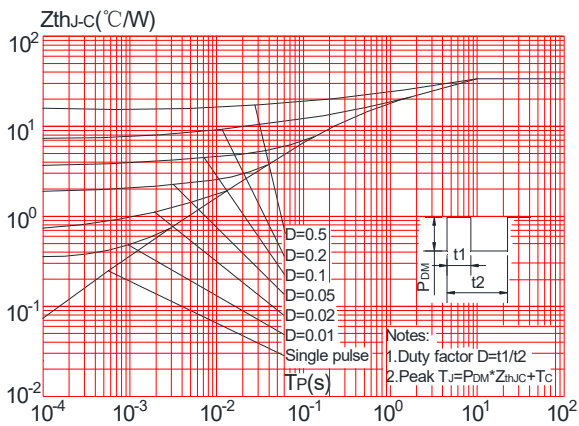
**Figure 9:** Maximum Safe Operating Area



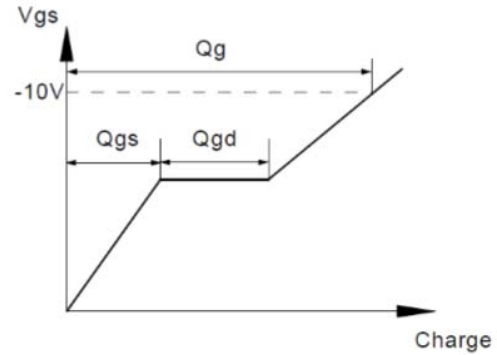
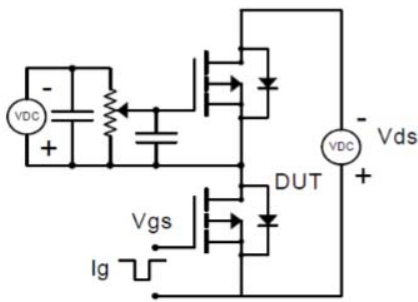
**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



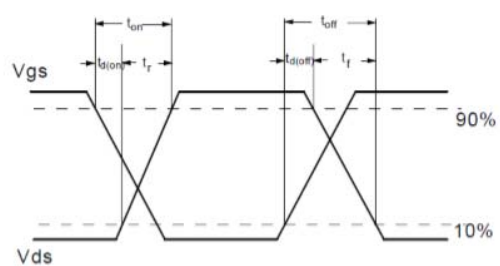
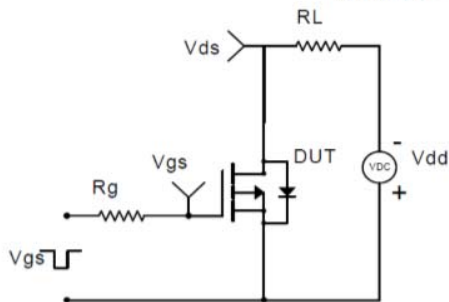
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



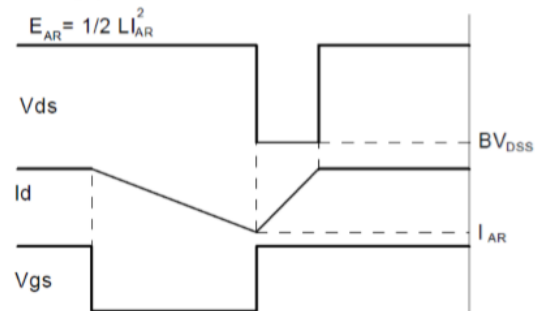
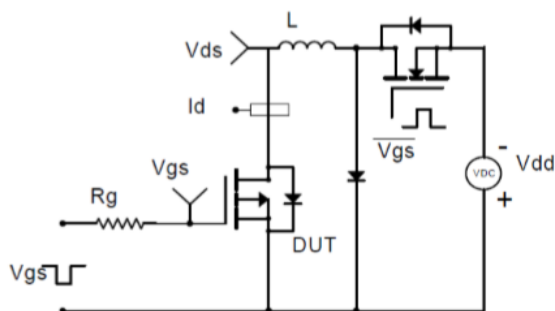
## Gate Charge Test Circuit & Waveform



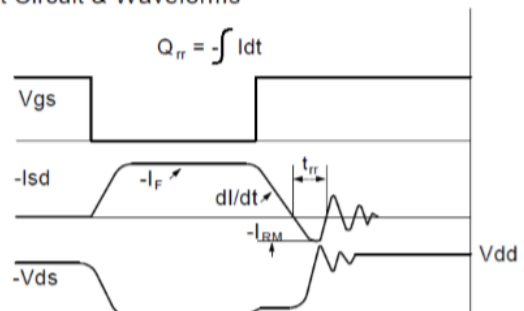
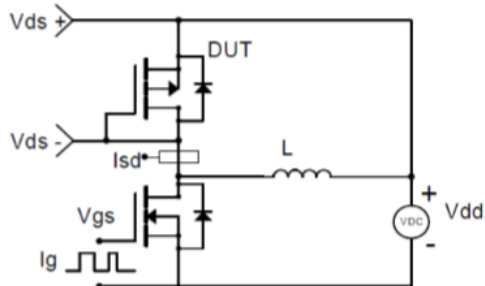
## Resistive Switching Test Circuit & Waveforms



## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

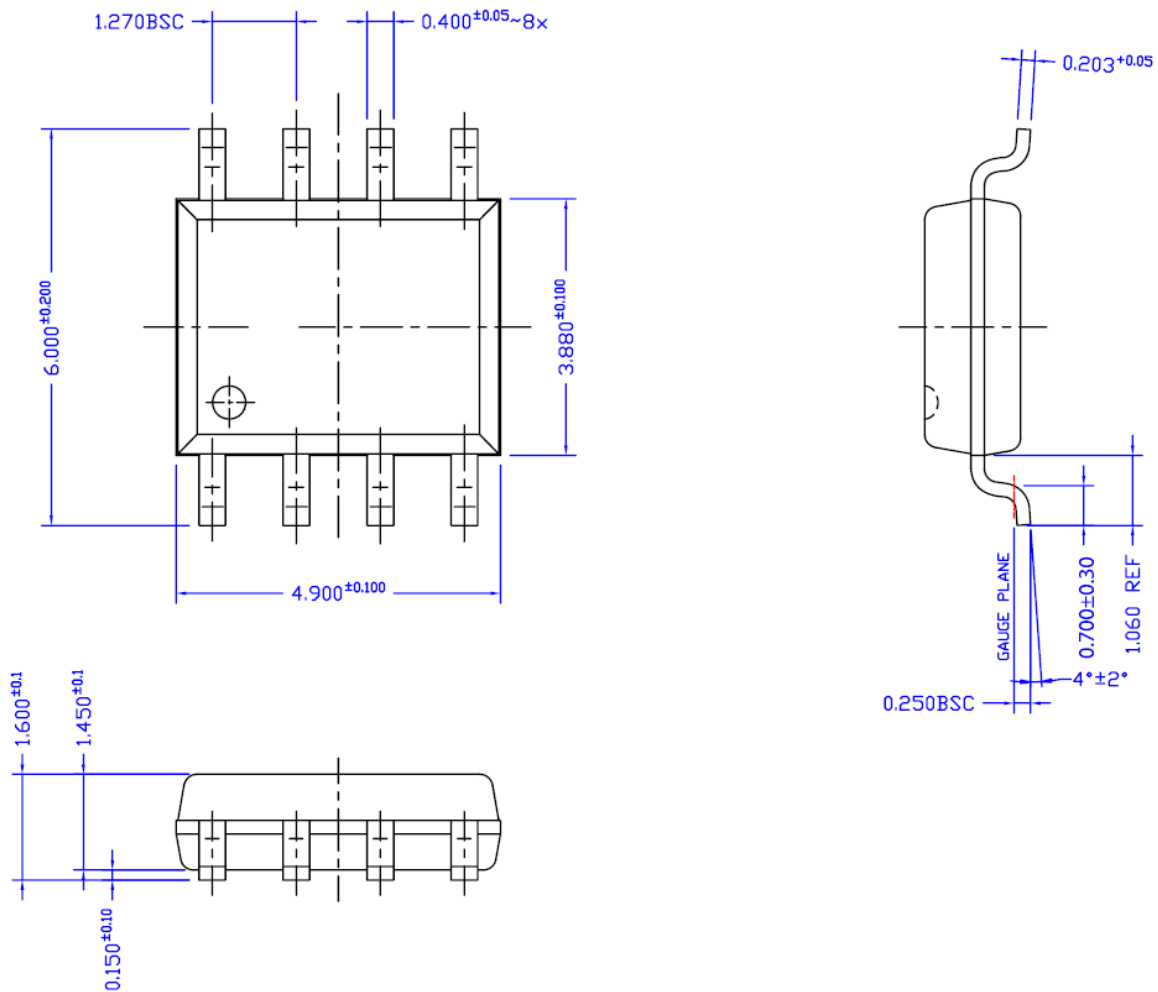


## Diode Recovery Test Circuit & Waveforms





## Package Mechanical Data




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