



## Description

### JMT N-channel Enhancement Mode Power MOSFET

#### Features

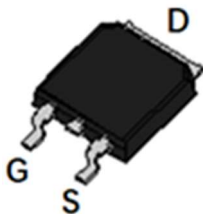
- 60V,50A  
 $R_{DS(ON)} < 17m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 25m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

- Load Switch
- PWM Application
- Power management



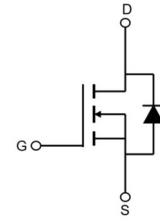
*100% UIS TESTED!*  
*100% ΔVds TESTED!*



TO-252(DPAK) top view



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMTK50N06B	JMTK50N06B	TAPING	TO-252	13inch	2500	25000

## Absolute Maximum Ratings (T<sub>C</sub>=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage	60	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	50
		T <sub>C</sub> = 100°C	33
I <sub>DM</sub>	Pulsed Drain Current <sup>note1</sup>	200	A
EAS	Single Pulsed Avalanche Energy <sup>note2</sup>	64	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	89
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	1.69	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +175	°C



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> = 0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.6	2.5	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	12	17	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	16	25	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> =0V, f = 1.0MHz	-	2900	-	pF
C <sub>oss</sub>	Output Capacitance		-	140	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	124	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	50	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	6	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	15	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =25V, I <sub>D</sub> =30A, R <sub>G</sub> = 1.8Ω, V <sub>GS</sub> =10V	-	7.4	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	5.1	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	28.2	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	5.5	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> =30A	-	-	1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =30A, dI/dt=100A/μs	-	28	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	40	-	nC

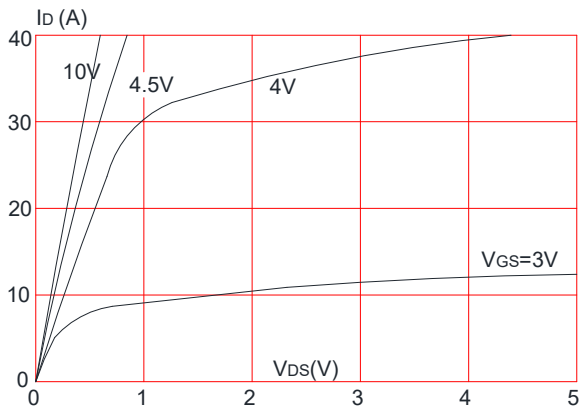
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=16A

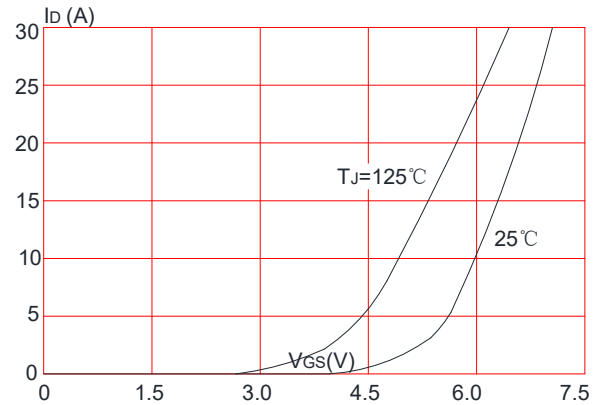
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



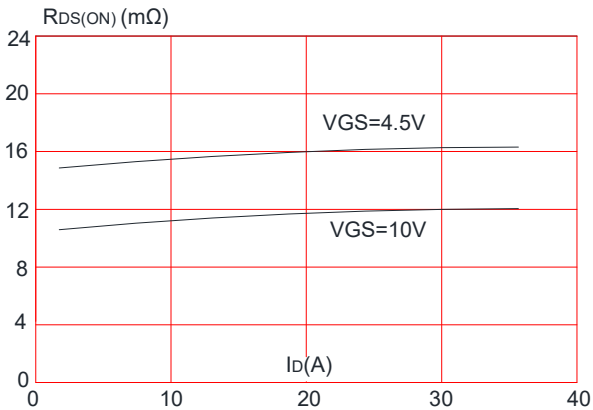
**Figure 1: Output Characteristics**



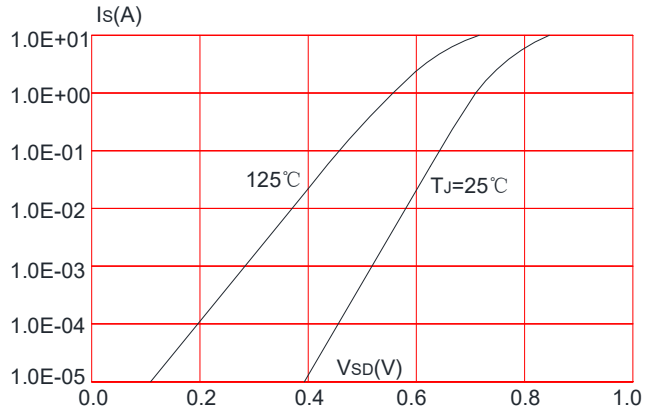
**Figure 2: Typical Transfer Characteristics**



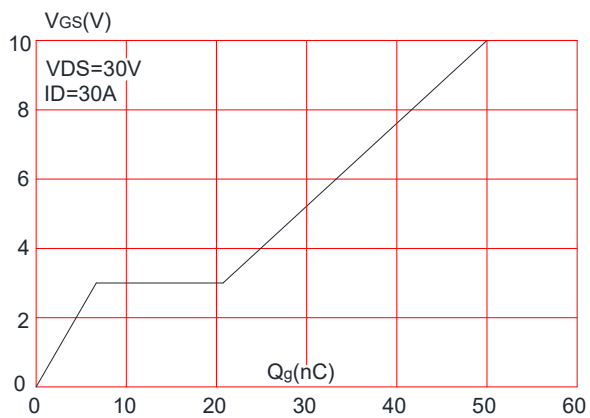
**Figure 3: On-resistance vs. Drain Current**



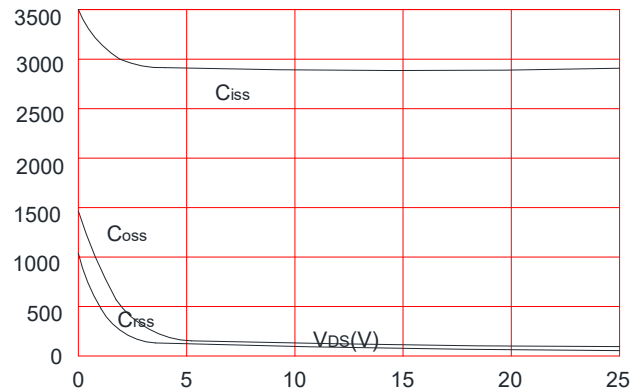
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**

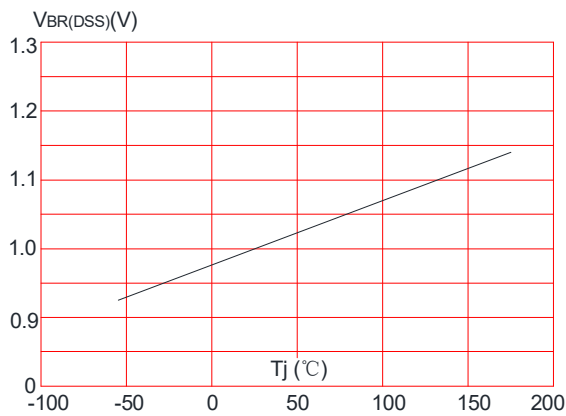


**Figure 6: Capacitance Characteristics**

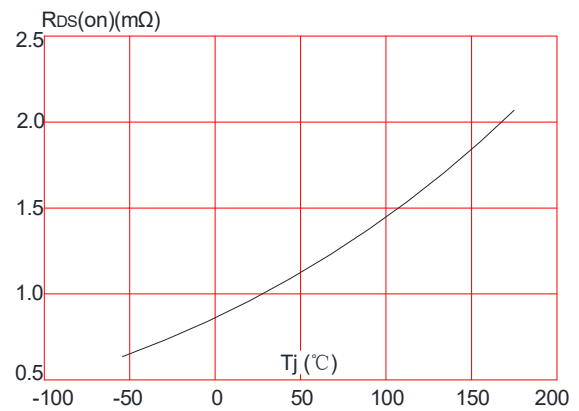




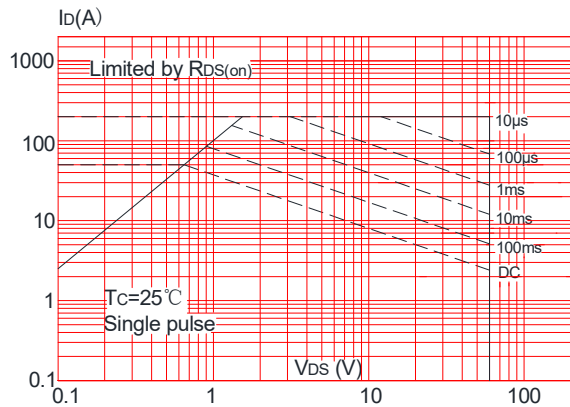
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



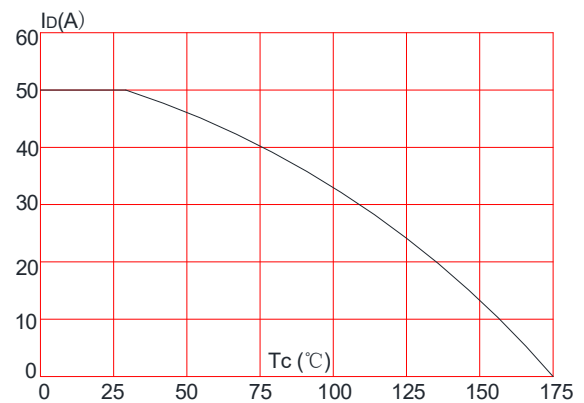
**Figure 8:** Normalized on Resistance vs. Junction Temperature



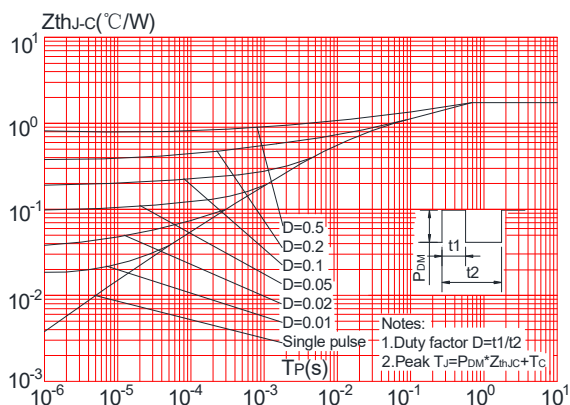
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## Test Circuit

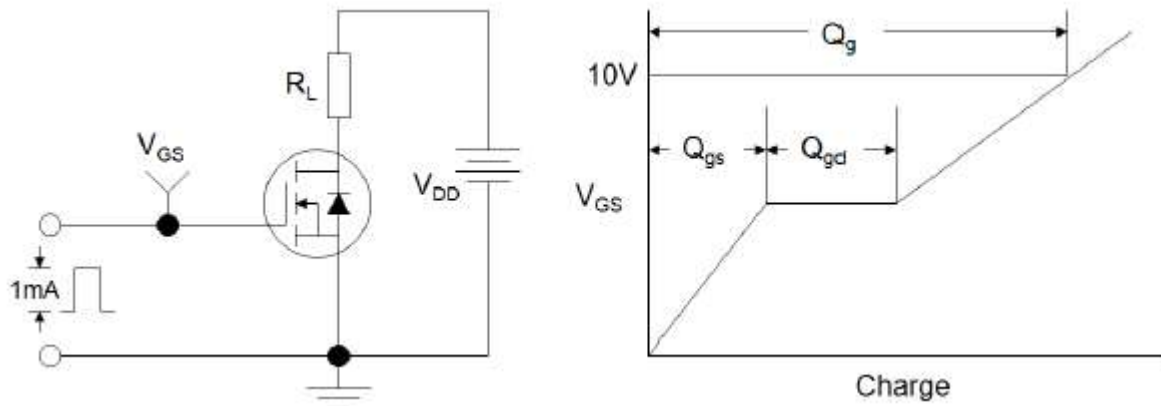


Figure 1: Gate Charge Test Circuit & Waveform

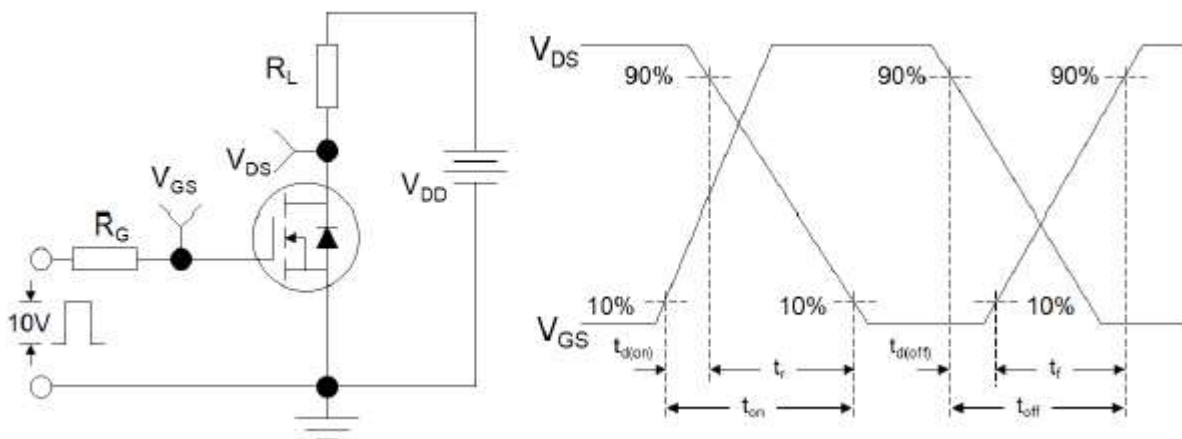


Figure 2: Resistive Switching Test Circuit & Waveforms

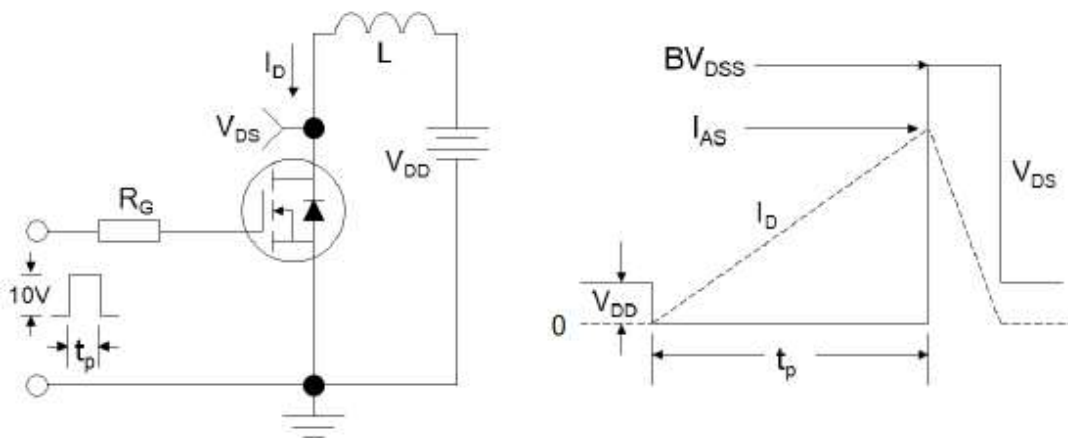
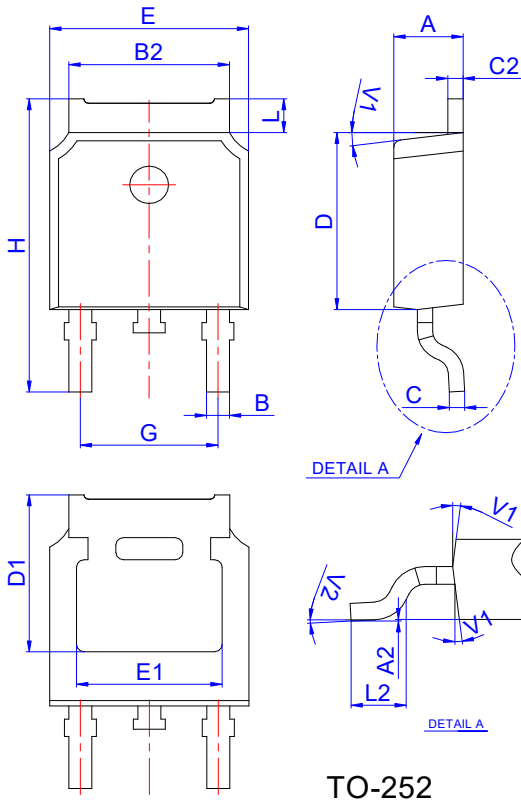


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

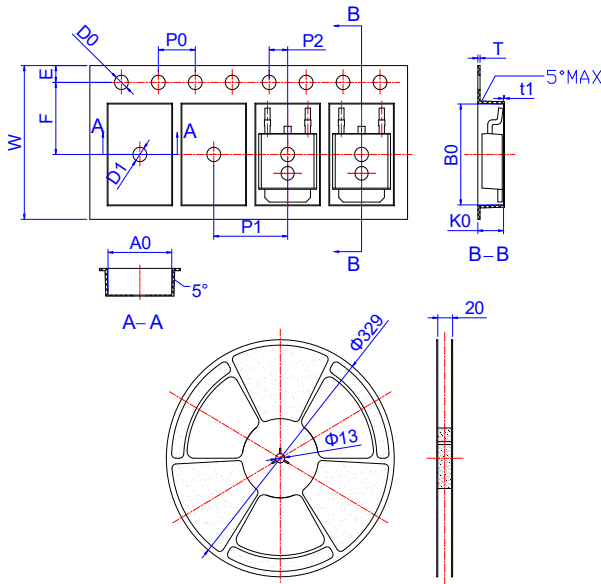


## Package Mechanical Data



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

## Reel Specification-TO-252




Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583



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