



Description

JMC Super Junction N-channel MOSFET

Features

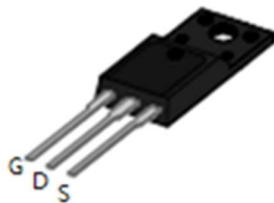
- $V_{DS}=650V$, $I_D=7A$
 $R_{DS(ON)} < 0.65\Omega @ V_{GS} = 10V$
- Multi-Epi process SJ-MOSFET
- Smart design in high voltage technology
- Ultra lower on-resistance
- Fast switching
- Ultra low gate charge
- Low reverse recovery charge

Application

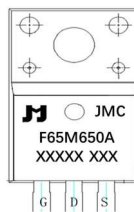
- Power factor correction (PFC)
- Switched mode power supplies (SMPS)
- Uninterruptible power supply (UPS)



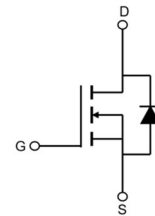
100% UIS TESTED!
100% ΔV_{ds} TESTED!



TO-220F top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	TUBE (PCS)	Inner Box (PCS)	Per Carton (PCS)
JMCF65M650A	JMCF65M650A	TUBE	TO-220F	50	1,000	8,000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	650	V
V_{GSS}	Gate-Source Voltage	± 30	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	7
		$T_C = 100^\circ C$	4.6
I_{DM}	Pulsed Drain Current ^{note1}	28	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	324.9	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	31.4
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.98	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	80	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	650	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =650V, V _{GS} = 0V, T _C = 25°C	-	-	1	μA
		V _{DS} =650V, V _{GS} = 0V, T _C = 125°C	-	-	100	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±30V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	2.0	3.0	4.0	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} =10V, I _D =3.5A	-	0.56	0.65	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =50V, V _{GS} = 0V, f = 1.0MHz	-	435	-	pF
C _{oss}	Output Capacitance		-	28	-	pF
C _{rss}	Reverse Transfer Capacitance		-	3.3	-	pF
Q _g	Total Gate Charge	V _{DS} =480V, I _D =7A, V _{GS} =10V	-	11	-	nC
Q _{gs}	Gate-Source Charge		-	3.5	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	5	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DS} =380V, I _D =3.5A, V _{GS} =10V, R _G =6.8Ω	-	8	-	ns
t _r	Turn-on Rise Time		-	7	-	ns
t _{d(off)}	Turn-off Delay Time		-	58	-	ns
t _f	Turn-off Fall Time		-	9	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	7	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	28	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =7A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S =3.5A, di/dt=100A/μs	-	210	-	ns
Q _{rr}	Reverse Recovery Charge		-	0.85	-	μC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J = 25°C, V_{DD} = 50V, V_G=10V, L=20mH, I_{AS} =5.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Typical Performance Characteristics

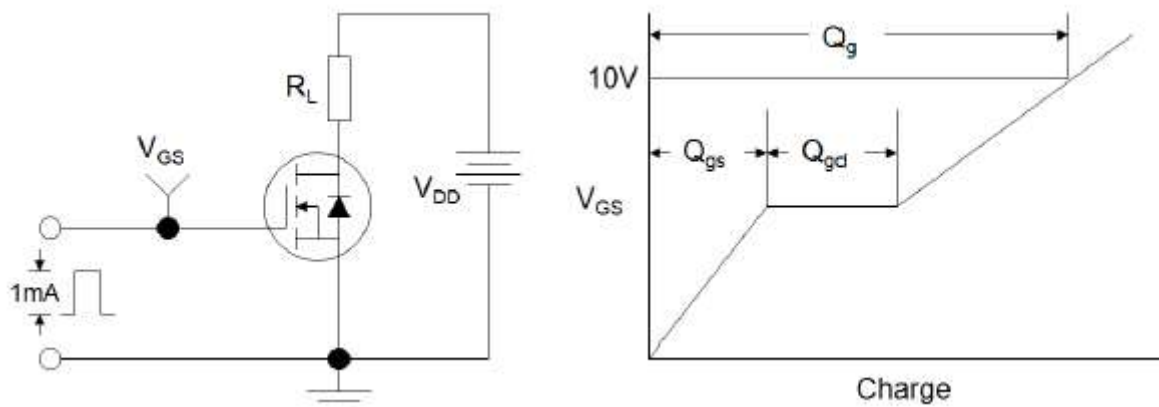


Figure1: Gate Charge Test Circuit & Waveform

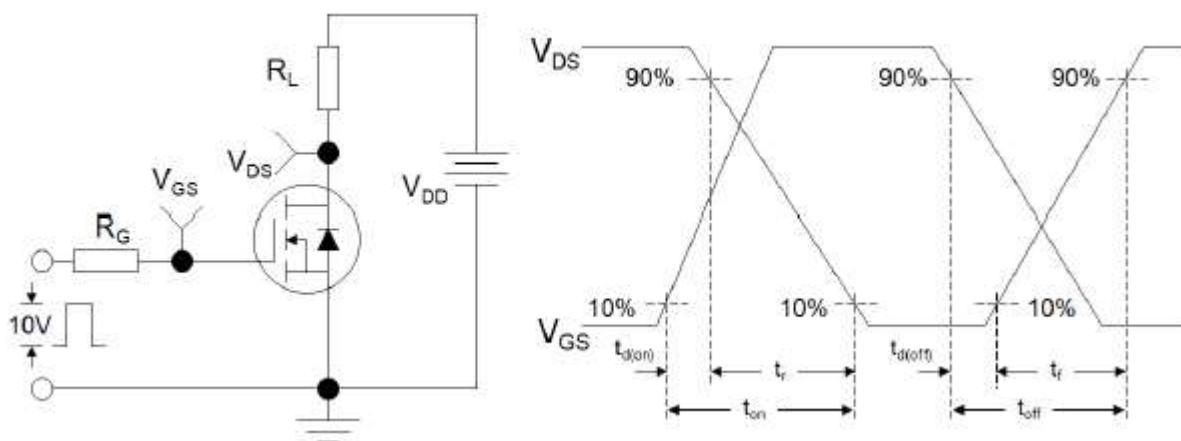


Figure 2: Resistive Switching Test Circuit & Waveforms

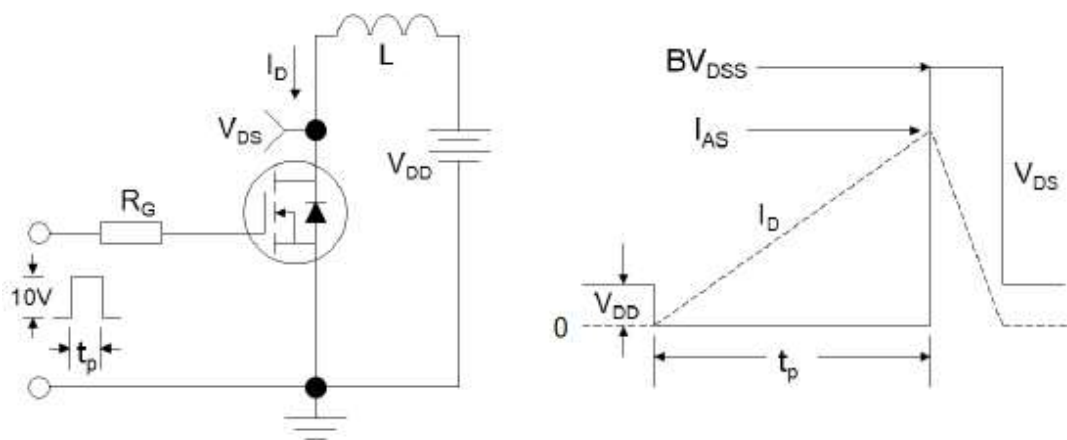
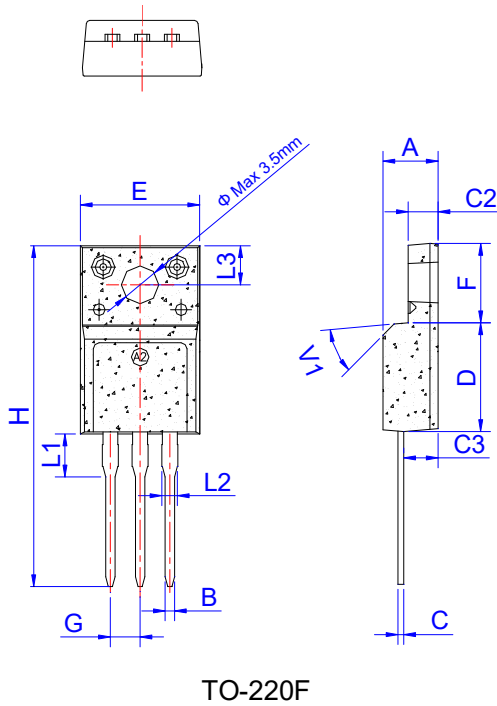


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data




Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.50		4.90	0.177		0.193
B	0.74	0.80	0.83	0.029	0.031	0.033
C	0.47		0.65	0.019		0.026
C2	2.45		2.75	0.096		0.108
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.80		10.4	0.386		0.410
F	6.40		6.80	0.252		0.268
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.63			0.143	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	

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