



LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8644

Digital Crosspoint Switch

Datasheet



1. Features

- DC to 3.4Gbps per port NRZ data rate
- Programmable receive equalization
- Programmable CML output levels
- 50Ω on-chip I/O termination
- I2C slave control interface
- ESD rating: HBM at ±7kV

2. General Description

The LT8644 is a 16×16 digital crosspoint switch, with 16 differential CML compatible inputs and 16 differential CML outputs. The LT8644 is optimized for nonreturn-to-zero

(NRZ) signaling with data rates of up to 3.4Gbps per port. Each port offers programmable level of input equalization and programmable output swing. The LT8644 supports independent channel switching through the serial control interface. The LT8644 has low latency and very low channel-to-channel skew. An I2C interface is used to control the device and provide access to advanced features.

3. Applications

- Fiber optic network switching
- Digital video (HDMI, DVI)
- Data storage networks



Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8644	-40° C to +85° C	TQFP100 (14*14)	Tray



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5. Revision History

Version	Owner	Content	Date
Preliminary	Y S	Initial datasheet creation	03/07/2013
Preliminary	Y S	Update electrical character data	09/10/2014
Preliminary	N W	Update package information	09/11/2014
R1.0	DY Z	Update power dissipation	05/12/2014
R1.1	N W	Check package information	03/13/2015
R1.2		Modify the format of the document	05/03/2017

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6. Pinning Information

6.1 Pin Configuration

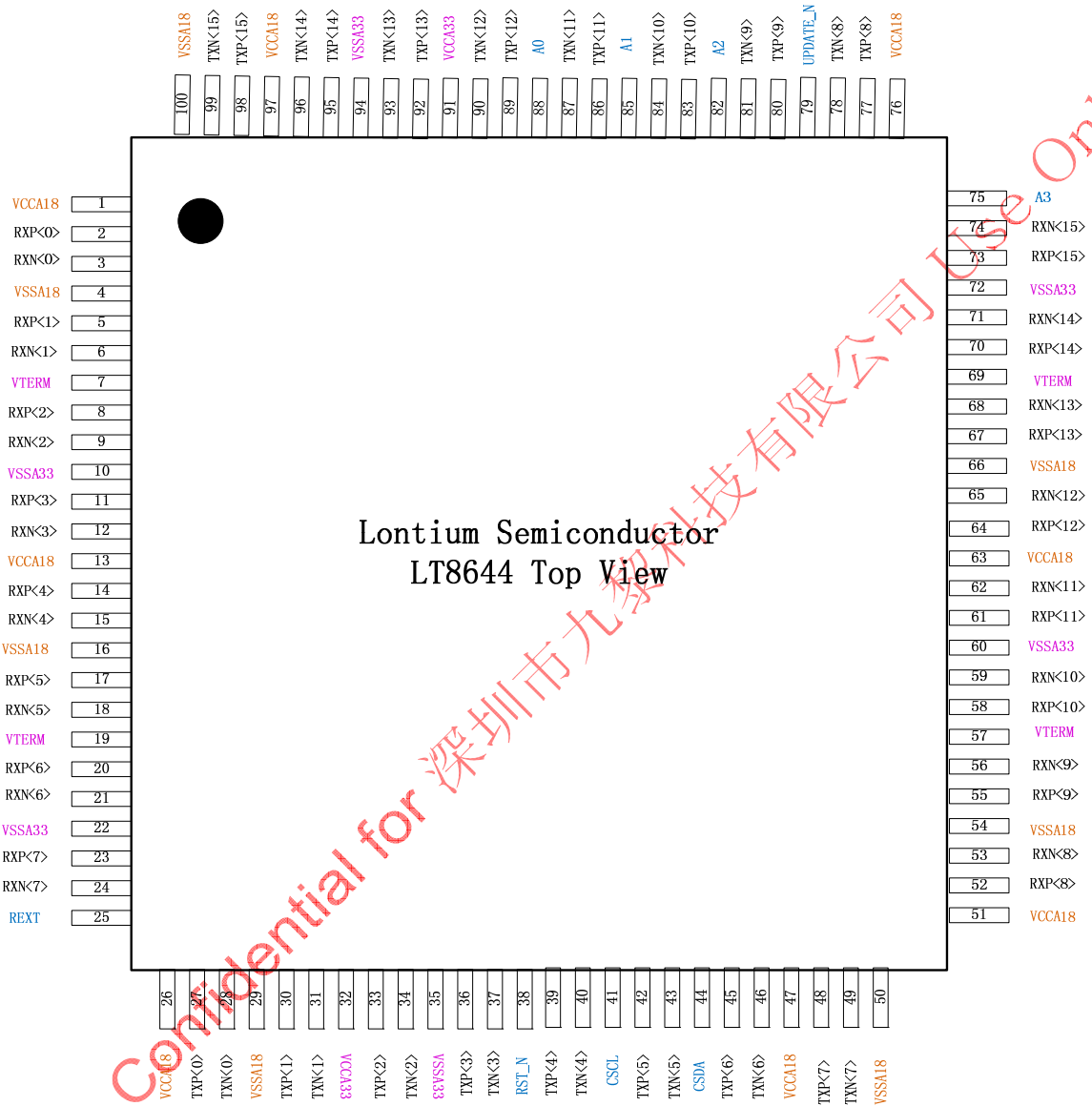


Figure 6.1.1 Pin Assignment

6.2 Pin Description

Table 6.2.1 Pin Description

Symbol	Number	Type	Description	Note
CML Input Signals				
RXP<0>	2	CML input	Positive high speed Input	
RXN<0>	3	CML input	Negative high speed Input	
RXP<1>	5	CML input	Positive high speed Input	
RXN<1>	6	CML input	Negative high speed Input	
RXP<2>	8	CML input	Positive high speed Input	
RXN<2>	9	CML input	Negative high speed Input	
RXP<3>	11	CML input	Positive high speed Input	
RXN<3>	12	CML input	Negative high speed Input	
RXP<4>	14	CML input	Positive high speed Input	
RXN<4>	15	CML input	Negative high speed Input	
RXP<5>	17	CML input	Positive high speed Input	
RXN<5>	18	CML input	Negative high speed Input	
RXP<6>	20	CML input	Positive high speed Input	
RXN<6>	21	CML input	Negative high speed Input	
RXP<7>	23	CML input	Positive high speed Input	
RXN<7>	24	CML input	Negative high speed Input	
RXP<8>	52	CML input	Positive high speed Input	
RXN<8>	53	CML input	Negative high speed Input	
RXP<9>	55	CML input	Positive high speed Input	
RXN<9>	56	CML input	Negative high speed Input	
RXP<10>	58	CML input	Positive high speed Input	
RXN<10>	59	CML input	Negative high speed Input	
RXP<11>	61	CML input	Positive high speed Input	
RXN<11>	62	CML input	Negative high speed Input	
RXP<12>	64	CML input	Positive high speed Input	
RXN<12>	65	CML input	Negative high speed Input	
RXP<13>	67	CML input	Positive high speed Input	
RXN<13>	68	CML input	Negative high speed Input	
RXP<14>	70	CML input	Positive high speed Input	
RXN<14>	71	CML input	Negative high speed Input	
RXP<15>	73	CML input	Positive high speed Input	
RXN<15>	74	CML input	Negative high speed Input	
CML Output Signals				
TXP<0>	27	CML output	Positive high speed output	
TXN<0>	28	CML output	Negative high speed output	
TXP<1>	30	CML output	Positive high speed output	
TXN<1>	31	CML output	Negative high speed output	
TXP<2>	33	CML output	Positive high speed output	
TXN<2>	34	CML output	Negative high speed output	
TXP<3>	36	CML output	Positive high speed output	

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TXN<3>	37	CML output	Negative high speed output	
TXP<4>	39	CML output	Positive high speed output	
TXN<4>	40	CML output	Negative high speed output	
TXP<5>	42	CML output	Positive high speed output	
TXN<5>	43	CML output	Negative high speed output	
TXP<6>	45	CML output	Positive high speed output	
TXN<6>	46	CML output	Negative high speed output	
TXP<7>	48	CML output	Positive high speed output	
TXN<7>	49	CML output	Negative high speed output	
TXP<8>	77	CML output	Positive high speed output	
TXN<8>	78	CML output	Negative high speed output	
TXP<9>	80	CML output	Positive high speed output	
TXN<9>	81	CML output	Negative high speed output	
TXP<10>	83	CML output	Positive high speed output	
TXN<10>	84	CML output	Negative high speed output	
TXP<11>	86	CML output	Positive high speed output	
TXN<11>	87	CML output	Negative high speed output	
TXP<12>	89	CML output	Positive high speed output	
TXN<12>	90	CML output	Negative high speed output	
TXP<13>	92	CML output	Positive high speed output	
TXN<13>	93	CML output	Negative high speed output	
TXP<14>	95	CML output	Positive high speed output	
TXN<14>	96	CML output	Negative high speed output	
TXP<15>	98	CML output	Positive high speed output	
TXN<15>	99	CML output	Negative high speed output	
I2C Slave Address				
A0	88	LVTTL input	I2C slave address bit0 (LSB)	Internal weak pull-down
A1	85	LVTTL input	I2C slave address bit1	Internal weak pull-down
A2	82	LVTTL input	I2C slave address bit2	Internal weak pull-down
A3	75	LVTTL input	I2C slave address bit3 (MSB)	Internal weak pull-down
Miscellaneous				
VCCA33	32, 91	Power	3.3V±10%	
VSSA33	10,22,35,60,72,94	Ground	Analog ground pin	
VTERM	7,19,57,69	Power	Termination power pin. This pin provides bias for ODTs.	
VCCA18	1,13,26,47,51,63,76,97	Power	1.8V±10%	
VSSA18	4,16,29,50,54,66,100	Ground	Analog ground pins	
REXT	25	Analog I/O	Current sense port used to provide an accurate current reference for bias circuits. Connecting	

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			this pin through a 2k resistor ($\pm 1\%$) to VSSA33 is recommended.	
RST_N	38	LVTTL input	Chip reset pin, active low. With internal weak pull up.	Internal pull-up weak
UPDATE_N	79	LVTTL input	Synchronous update, active low.	Internal pull-up weak
CSDA	44	Open drain	Configuration I2C SDA line.	
C_SCL	41	Open drain	Configuration I2C SCL line.	

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7. Function Block Diagram

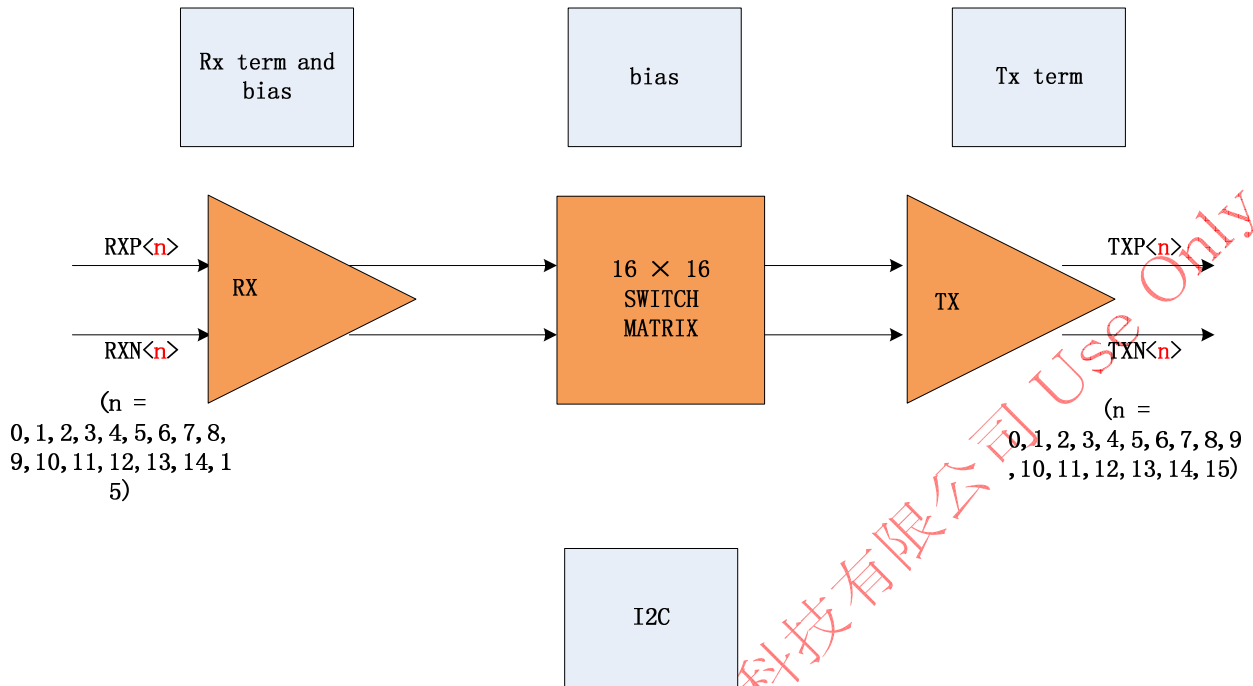


Figure 7.1 Function Block Diagram

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8. Electrical Characteristics

Table 8.1 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
	VCCA33	Normal Operation	3.0	3.3	3.6	V
	VCCA18	Normal Operation	1.6	1.8	2.0	V
	IVCCA33	Normal Operation			338	mA
		Power Down			0	mA
	IVCCA18	Normal Operation			275	mA
		Power Down			0	mA
CML Inputs (Source Side)						
Differential Input Voltage Swing(DC)	VID		150	1000	1400	mVP-P
Common-Mode Input Voltage(DC)	VICM			VCCA33-0.25		V
Input Resistance	RI	Single-ended	45	50	55	Ω
CML Outputs (Sink Side)						
Standby Output Voltage	VOFF	Power Down	VCCA33-10	VCCA33+10		mV
Differential Output-Voltage Swing(DC)	VOD	50 ohm Load	800	1000	1200	mVP-P
Output-Voltage High	VODH	Single-Ended		VCCA33+10		mV
Output-Voltage Low	VODL	Single-Ended	VCCA33-1	VCCA33-0.05		V
Common-Mode Output Voltage	VOCM	50 ohm Load	VCCA33-0.25			V
Rise/Fall Time	TR /TF	20% ~ 80%	80	130	200	ps
LVTTTL Inputs						
LVTTTL Input High Voltage	VIH		2.0			V
LVTTTL Input Low Voltage	VIL				0.8	V
LVTTTL Outputs						
LVTTTL Output High Voltage	VOH		2.4			V
LVTTTL Output Low Voltage	VOL				0.4	V
I2C Configuration I/O						
I2C Input High Voltage	VIHI2C		2.0			V
I2C Input Low Voltage	VILI2C				0.8	V
I2C Output Low Voltage (Open-Drain)	VOLI2C	RLOAD = 4.7k Ω to 3.3V			0.4	V
Analog Configuration Inputs						
Analog Input Voltage Range	VIA		0		3.3	V

8.1 DC Specifications

Under normal operating conditions unless otherwise specified.

Table 8.1.1 DC Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
V _{ID}	TMDS differential input voltage, single ended amplitude						mV
I _{CC18}	Normal Operating current	TMDS CLK=27M	1.8V				mA
I _{CC33}			3.3V				mA
I _{CC18}		TMDS CLK=74.25M	1.8V		356		mA
I _{CC33}			3.3V		225		mA
I _{CC18}		TMDS CLK=148.5M	1.8V		370		mA
I _{CC33}			3.3V		225		mA
I _{CC18}		TMDS CLK=296M	1.8V		395		mA
I _{CC33}			3.3V		296		mA

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9. Packaging(TQFP100 (14x14x1.0))

The LT8644 can be packaged in TQFP100 14x14x1.0.

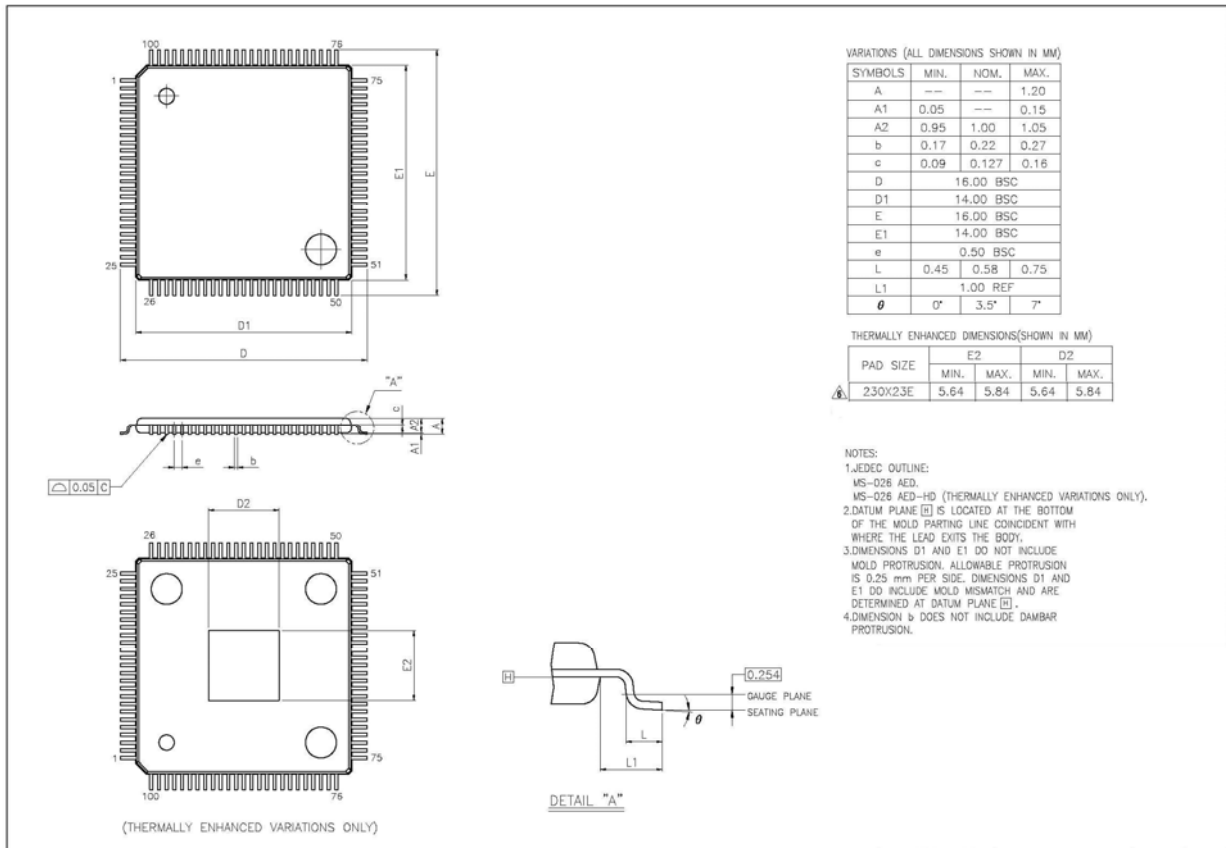


Figure 9.1 TQFP100 (14x14x1.0) Package Diagrams

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