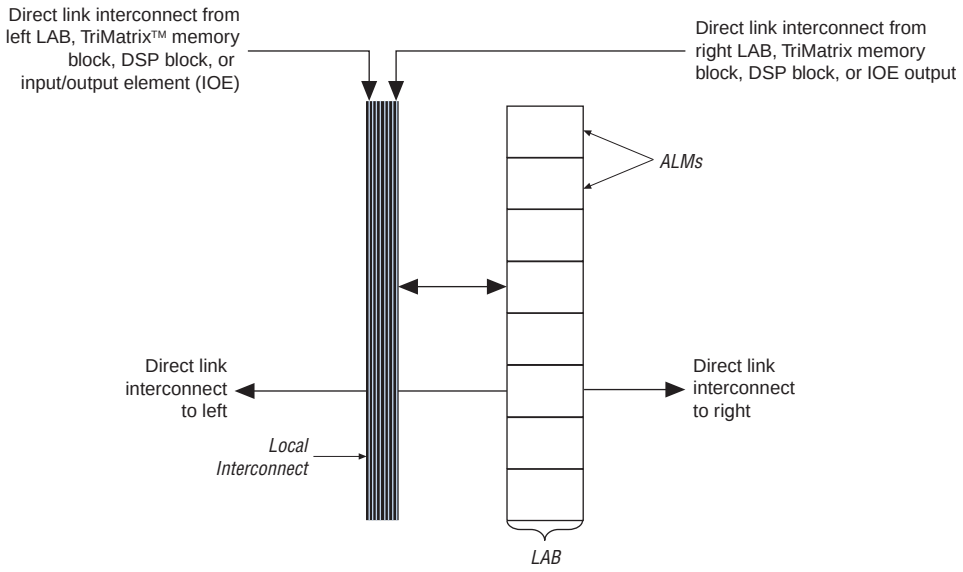
Figure 2–33 shows the direct link connection.

*Figure 2–33. Direct Link Connection*




## LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–34. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous

### *Carry Chain*

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions, such as LPM functions, automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically, allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. The other half of the ALMs in the LAB is available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB will carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB will carry into the bottom half of the ALMs in the next LAB within the column. Every other column of the LABs are top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to "MultiTrack Interconnect" on page 2–63 for more information on carry chain interconnect.

## Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) using a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–43 shows the ALM in shared arithmetic mode.

芯片详细信息

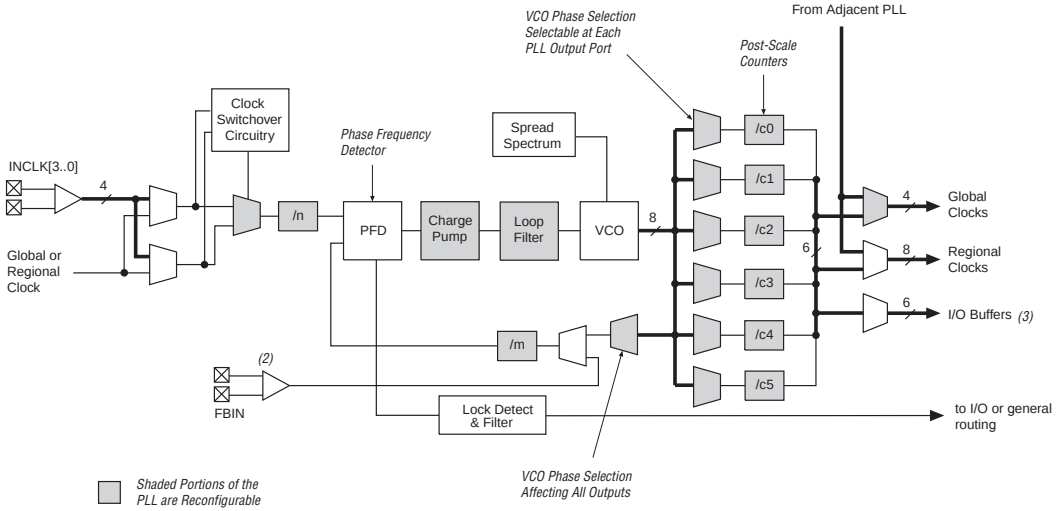
| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>EP3CLS100F484I7 | Rohs Code:<br>No | Part Life Cycle Code:<br>Active | Ihs Manufacturer:<br>INTEL CORP |
| Package Description:<br>23 X 23 MM, 1 MM PITCH, FBGA-484 | Reach Compliance Code:<br>compliant | ECCN Code:<br>3A991 | HTS Code:<br>8542.39.00.01 |
| Manufacturer:<br>Intel Corporation | Risk Rank:<br>5.27 | Clock Frequency-Max:<br>450 MHz | JESD-30 Code:<br>S-PBGA-B484 |
| Length:<br>23 mm | Number of CLBs:<br>100448 | Number of Inputs:<br>278 | Number of Logic Cells:<br>100448 |
| Number of Outputs:<br>278 | Number of Terminals:<br>484 | Operating Temperature-Max:<br>100 °C | Operating Temperature-Min:<br>-40 °C |
| Organization:<br>100448 CLBS | Package Body Material:<br>PLASTIC/EPOXY | Package Code:<br>BGA | Package Equivalence Code:<br>BGA484,22X22,40 |
| Package Shape:<br>SQUARE | Package Style:<br>GRID ARRAY | Power Supplies:<br>1.2,1.2/3.3,2.5 V | Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY |
| Qualification Status:<br>Not Qualified | Seated Height-Max:<br>2.4 mm | Subcategory:<br>Field Programmable Gate Arrays | Supply Voltage-Max:<br>1.25 V |
| Supply Voltage-Min:<br>1.15 V | Supply Voltage-Nom:<br>1.2 V | Surface Mount:<br>YES | Technology:<br>CMOS |
| Temperature Grade:<br>INDUSTRIAL | Terminal Form:<br>BALL | Terminal Pitch:<br>1 mm | Terminal Position:<br>BOTTOM |
| Width:<br>23 mm | | | |

| | | |
|---|---|---|
| 产品种类: | FPGA - 现场可编程门阵列 | ☑ |
| RoHS: | N | |
| 产品: | Cyclone III LS | ☐ |
| 系列: | Cyclone III EP3CLS100 | ☐ |
| 逻辑元件数量: | 100448 LE | ☐ |
| 自适应逻辑模块 - ALM: | - | ☐ |
| 嵌入式内存: | 4.25 Mbit | ☐ |
| 输入/输出端数量: | 294 I/O | ☐ |
| 工作电源电压: | 1.15 V to 1.25 V | ☐ |
| 最小工作温度: | - 40 C | ☐ |
| 最大工作温度: | + 85 C | ☐ |
| 安装风格: | SMD/SMT | ☐ |
| 封装 / 箱体: | FBGA-484 | ☐ |
| 封装: | Tray | ☐ |
| 商标: | Intel / Altera | |
| 最大工作频率: | 274 MHz | |
| 湿度敏感性: | Yes | |
| 逻辑数组块数量——LAB: | 6278 LAB | |
| 产品类型: | FPGA - Field Programmable Gate Array | |
| 工厂包装数量: | 60 | |
| 子类别: | Programmable Logic ICs | |
| 总内存: | 4451328 bit | |
| 商标名: | Cyclone III | |
| 零件号别名: | 972406 | |

## Enhanced PLLs

Stratix II GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2–74 shows a diagram of the enhanced PLL.

***Figure 2–74. Stratix II GX Enhanced PLL*** *Note (1)*




*Notes to Figure 2–74:*

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.
(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.
(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.
(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

## Fast PLLs

Stratix II GX devices contain up to four fast PLLs with high-speed serial interfacing ability. The fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2–75 shows a diagram of the fast PLL.