5. DSP Blocks in Stratix III Devices

SIII51005-1.7

Introduction

The Stratix® III family of devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications. These DSP blocks of the Altera® Stratix device family are the third generation of hardwired, fixed function silicon blocks dedicated to maximizing signal processing capability, ease of use, and lowest silicon cost.

Many complex systems such as WiMAX, 3GPP WCDMA, high-performance computing (HPC), voice over Internet protocol (VoIP), H.264 video compression, medical imaging, and HDTV use sophisticated digital signal processing techniques, and this typically requires a large number of mathematical computations. Stratix III devices are ideally suited as the DSP blocks consist of a combination of dedicated elements that perform multiplication, addition, subtraction, accumulation, summation, and dynamic shift operations. Along with the high-performance Stratix III soft logic fabric and TriMatrix™ memory structures, you can configure these blocks to build sophisticated fixed-point and floating-point arithmetic functions. These can be manipulated easily to implement common larger computationally intensive subsystems such as finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

DSP Block Overview

Each Stratix III device has two to seven columns of DSP blocks that implement multiplication, multiply-add, multiply-accumulate (MAC), and dynamic shift functions efficiently. The logical functionality of the Stratix III DSP block is a superset of the previous generation of the DSP block found in Stratix and Stratix II devices.

Architectural highlights of the Stratix III DSP block include:

- High-performance, power-optimized, fully registered and pipelined multiplication operations
- Natively supported 9-bit, 12-bit, 18-bit, and 36-bit wordlengths
- Natively supported 18-bit complex multiplications
- Efficiently supported floating-point arithmetic formats (24-bit for single precision and 53-bit for double precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently
- Cascading 18-bit input bus to form tap-delay line for filtering applications
- Cascading 44-bit output bus to propagate output results from one block to the next block without external logic support
- Rich and flexible arithmetic rounding and saturation units

The second-stage and output registers are triggered by the positive edge of the clock signal and are cleared on power up. The following DSP block signals control the output registers within the DSP block:

- `clock[3..0]`
- `ena[3..0]`
- `aclr[3..0]`

Operational Mode Descriptions

The various modes of operation are discussed below.

Independent Multiplier Modes

In independent input and output multiplier mode, the DSP block performs individual multiplication operations for general-purpose multipliers.

9-, 12-, and 18-Bit Multiplier

You can configure each DSP block multiplier for 9-, 12-, or 18-bit multiplication. A single DSP block can support up to eight individual 9 × 9 multipliers, six 12 × 12 multipliers, or up to four individual 18 × 18 multipliers. For operand widths up to 9 bits, a 9 × 9 multiplier is implemented. For operand widths from 10 to 12 bits, a 12 × 12 multiplier is implemented, and for operand widths from 13 to 18 bits, an 18 × 18 multiplier is implemented. This is done by the Quartus II software by zero-padding the LSBs. Figure 5–8, Figure 5–9, and Figure 5–10 show the DSP block in the independent multiplier operation mode.

Figure 5–8. 18-Bit Independent Multiplier Mode for Half-DSP Block

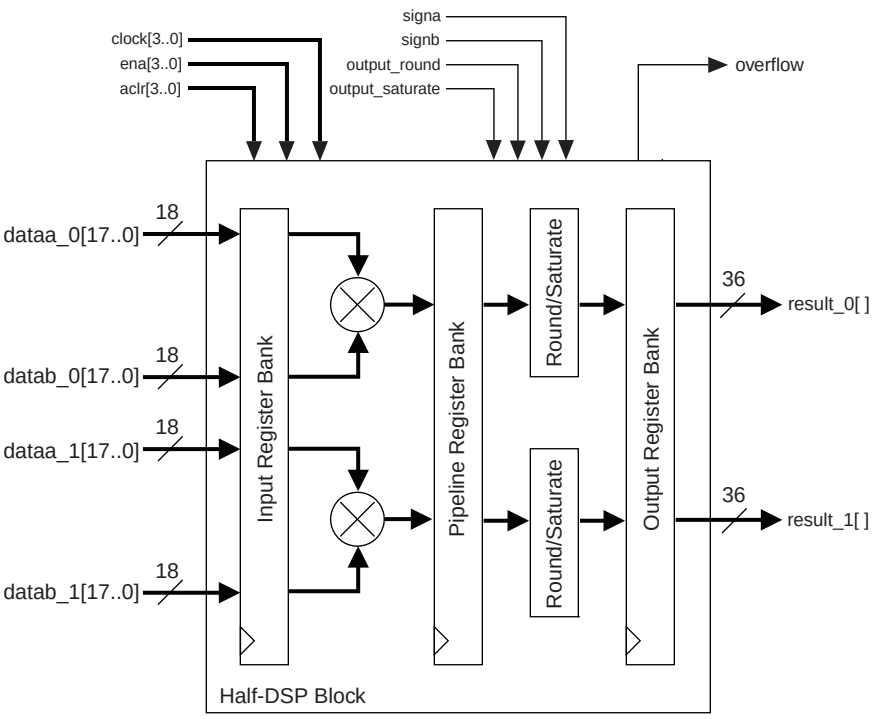
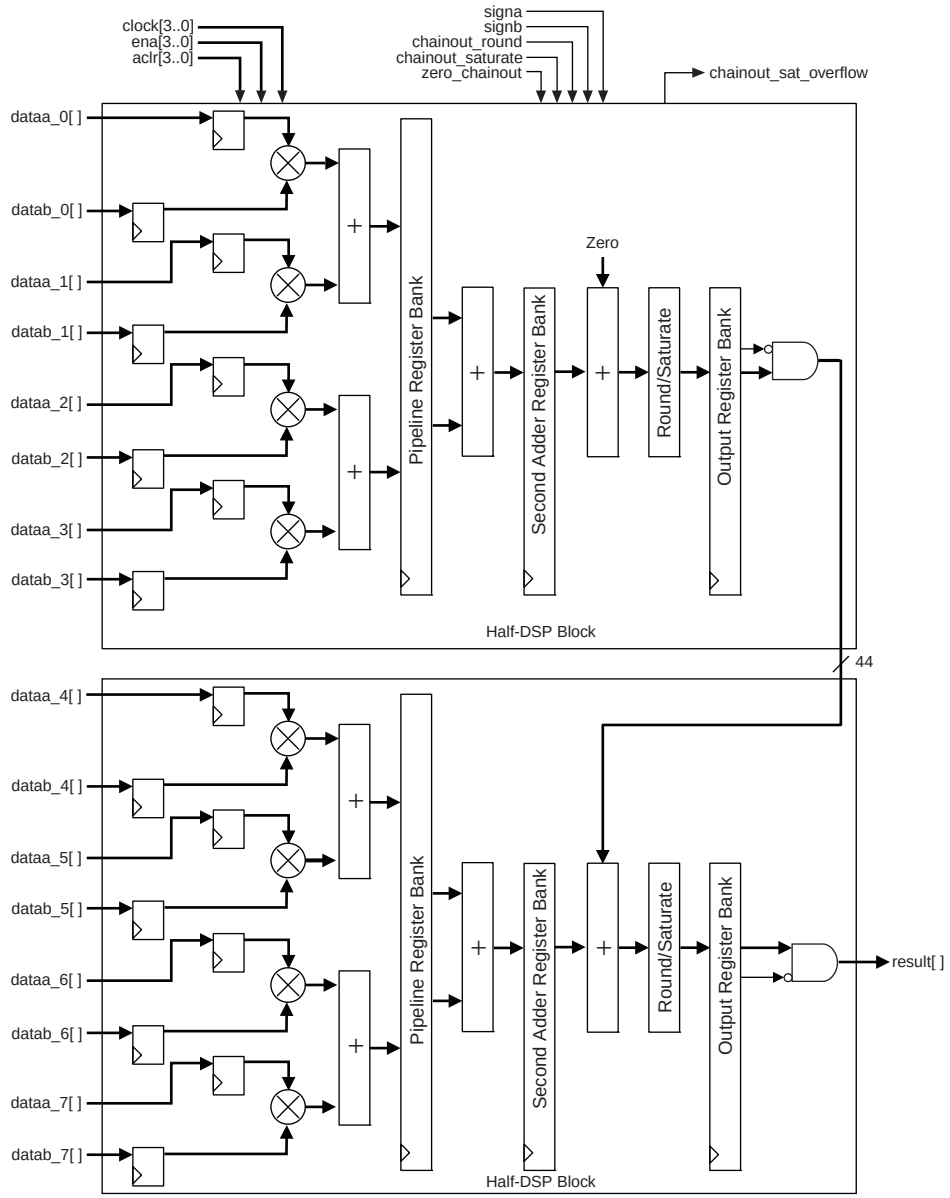


Figure 5–24. Semi-Parallel FIR Structure Using Chained Cascaded Summation



FFT Example

The Fast Fourier Transform (FFT) is a very common DSP function used to convert samples in the time domain to and from the frequency domain. A fundamental building block of the FFT is the FFT butterfly. FFTs are most efficient when operating on complex samples. You can use the Stratix III DSP block to form the core of a complex FFT butterfly very efficiently.

芯片详细信息

Manufacturer Part Number: EP3CLS100F484I7N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: LEAD FREE, FBGA-484	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.26	Clock Frequency-Max: 450 MHz	JESD-30 Code: S-PBGA-B484
JESD-609 Code: e1	Length: 23 mm	Moisture Sensitivity Level: 3	Number of CLBs: 100448
Number of Inputs: 278	Number of Logic Cells: 100448	Number of Outputs: 278	Number of Terminals: 484
Operating Temperature-Max: 100 °C	Operating Temperature-Min: -40 °C	Organization: 100448 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA484,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 260	Power Supplies: 1.2,1.2/3.3,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2.15 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: INDUSTRIAL
Terminal Finish: Tin/Silver/Copper (Sn/Ag/Cu)	Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 40	Width: 23 mm		

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Cyclone III LS	☐
系列:	Cyclone III EP3CLS100	☐
逻辑元件数量:	100448 LE	☐
自适应逻辑模块 - ALM:	-	☐
嵌入式内存:	4.25 Mbit	☐
输入/输出端数量:	294 I/O	☐
工作电源电压:	1.15 V to 1.25 V	☐
最小工作温度:	- 40 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-484	☐
封装:	Tray	☐
商标:	Intel / Altera	
最大工作频率:	274 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	6278 LAB	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	60	
子类别:	Programmable Logic ICs	
总内存:	4451328 bit	
商标名:	Cyclone III	
零件号别名:	970796	