Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–6 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–6. Multiplier Size & Configurations per DSP Block

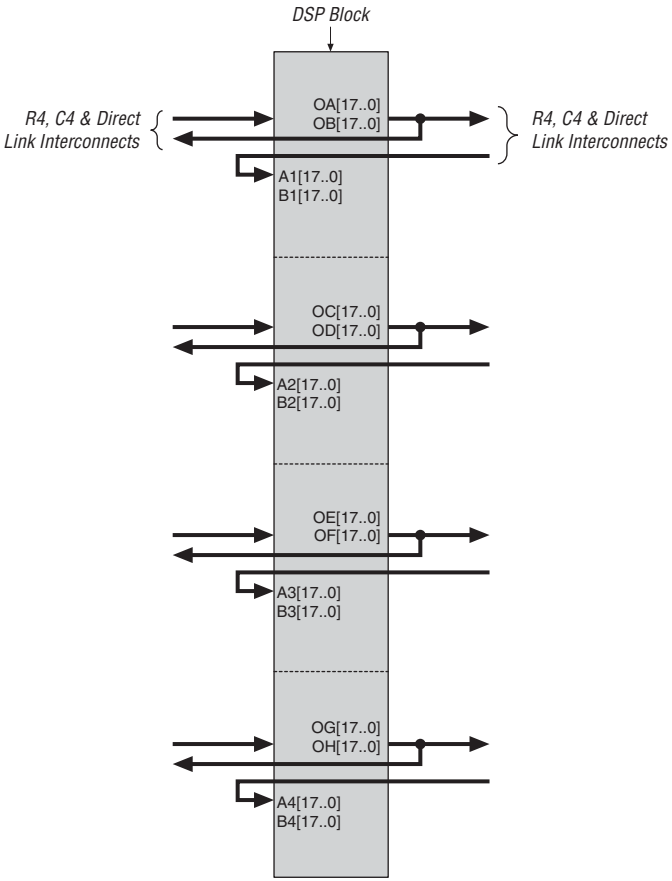
DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	-	Two 52-bit multiply-accumulate blocks	-
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	-
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	-

DSP Block Interface

Stratix II device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 2–29 and 2–30 show the DSP block interfaces to LAB rows.

Figure 2–29. DSP Block Interconnect Interface



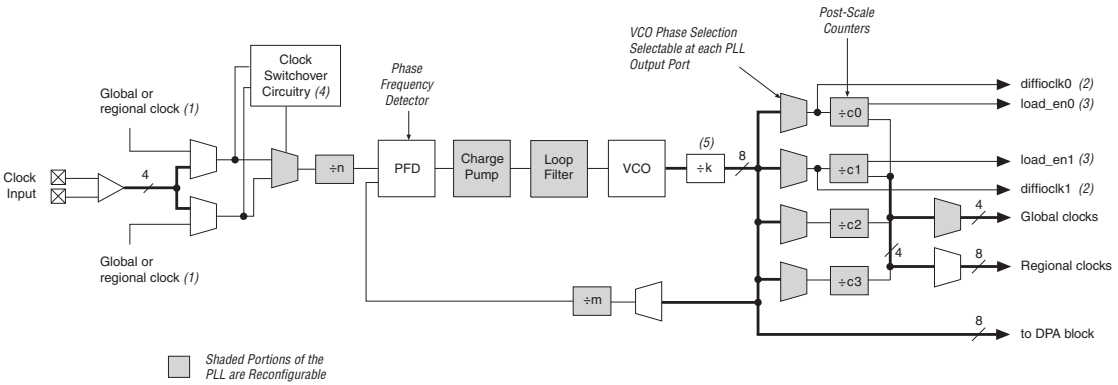
芯片详细信息

Manufacturer Part Number: EP3CLS100F484C8N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: LEAD FREE, FBGA-484	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.3	Clock Frequency-Max: 450 MHz	JESD-30 Code: S-PBGA-B484
JESD-609 Code: e1	Length: 23 mm	Moisture Sensitivity Level: 3	Number of CLBs: 100448
Number of Inputs: 278	Number of Logic Cells: 100448	Number of Outputs: 278	Number of Terminals: 484
Operating Temperature-Max: 85 °C	Organization: 100448 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA484,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 260
Power Supplies: 1.2,1.2/3.3,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.15 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V
Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: TIN SILVER COPPER
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 40
Width: 23 mm			

Fast PLLs

Stratix II devices contain up to eight fast PLLs with high-speed serial interfacing ability. Figure 2–45 shows a diagram of the fast PLL.

Figure 2–45. Stratix II Device Fast PLL *Notes (1), (2), (3)*



Notes to Figure 2–45:

(1) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES circuitry. Stratix II devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a differential I/O SERDES control signal.

(4) Stratix II fast PLLs only support manual clock switchover.

(5) If the design enables this ÷2 counter, then the device can use a VCO frequency range of 150 to 520 MHz.

See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on enhanced and fast PLLs. See "High-Speed Differential I/O with DPA Support" on page 2–96 for more information on high-speed differential I/O support.

I/O Structure

The Stratix II IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- On-chip driver series termination
- On-chip parallel termination
- On-chip termination for differential standards
- Programmable pull-up during configuration

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Cyclone III LS	☐
系列:	Cyclone III EP3CLS100	☐
逻辑元件数量:	100448 LE	☐
自适应逻辑模块 - ALM:	-	☐
嵌入式内存:	4.25 Mbit	☐
输入/输出端数量:	294 I/O	☐
工作电源电压:	1.15 V to 1.25 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-484	☐
封装:	Tray	☐
商标:	Intel / Altera	
最大工作频率:	274 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	6278 LAB	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	60	
子类别:	Programmable Logic ICs	
总内存:	4451328 bit	
商标名:	Cyclone III	
零件号别名:	970795	