One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs.

Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–36). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This feature provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Stratix II Performance and Logic Efficiency Analysis White Paper* for more information on the efficiencies of the Stratix II GX ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II GX ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. Each mode has 11 available inputs to the ALM (see Figure 2–35)—the eight data inputs from the LAB local interconnect; carry-in from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock,

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Cyclone III LS	☐
系列:	Cyclone III EP3CLS100	☐
逻辑元件数量:	100448 LE	☐
自适应逻辑模块 - ALM:	-	☐
嵌入式内存:	4.25 Mbit	☐
输入/输出端数量:	294 I/O	☐
工作电源电压:	1.15 V to 1.25 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-484	☐
封装:	Tray	☐
商标:	Intel / Altera	
最大工作频率:	274 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	6278 LAB	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	60	
子类别:	Programmable Logic ICs	
总内存:	4451328 bit	
商标名:	Cyclone III	
零件号别名:	970794	

芯片详细信息

Manufacturer Part Number: EP3CLS100F484C7N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: LEAD FREE, FBGA-484	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.26	Clock Frequency-Max: 450 MHz	JESD-30 Code: S-PBGA-B484
JESD-609 Code: e1	Length: 23 mm	Moisture Sensitivity Level: 3	Number of CLBs: 100448
Number of Inputs: 278	Number of Logic Cells: 100448	Number of Outputs: 278	Number of Terminals: 484
Operating Temperature-Max: 85 °C	Organization: 100448 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA484,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 260
Power Supplies: 1.2,1.2/3.3,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.15 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V
Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: Tin/Silver/Copper (Sn/Ag/Cu)
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 40
Width: 23 mm			

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Stratix II GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Stratix II GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix II GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

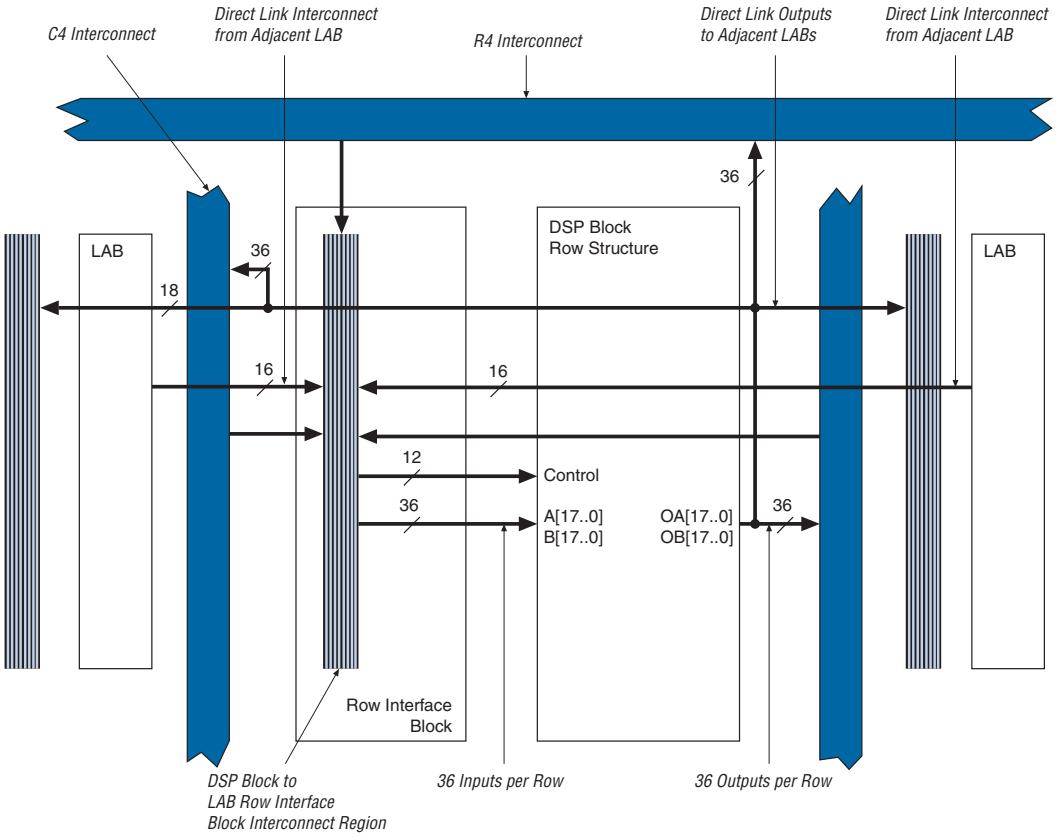
DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

Figure 2–60. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–23.

Refer to the *DSP Blocks in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on DSP blocks.