PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (CLK[15..0]) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	CLK pins, PLL outputs, or internal logic	CLK pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between CLKp pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

Table 2–10 shows the enhanced PLL and fast PLL features in Stratix II devices.

Table 2–10. Stratix II PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	$m/(n \times$ post-scale counter) (1)	$m/(n \times$ post-scale counter) (2)
Phase shift	Down to 125-ps increments (3), (4)	Down to 125-ps increments (3), (4)
Clock switchover	✓	✓ (5)
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	(6)
Number of feedback clock inputs	One single-ended or differential (7), (8)	

Notes to Table 2–10:
(1) For enhanced PLLs, *m* ranges from 1 to 256, while *n* and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix II devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Stratix II fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate txclkout.
(7) If the feedback input is used, you lose one (or two, if FBIN is differential) external clock output pin.
(8) Every Stratix II device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

芯片详细信息

Manufacturer Part Number:	Pbfree Code:	Rohs Code:	Part Life Cycle Code:
EP3C80U484I6N	✔ Yes	✔ Yes	Transferred
Ihs Manufacturer:	Package Description:	Reach Compliance Code:	Manufacturer:
ALTERA CORP	FBGA, BGA484,22X22,32	compliant	Altera Corporation
Risk Rank:	JESD-30 Code:	JESD-609 Code:	Length:
5.81	S-PBGA-B484	e1	19 mm
Number of Inputs:	Number of Logic Cells:	Number of Outputs:	Number of Terminals:
295	81264	295	484
Package Body Material:	Package Code:	Package Equivalence Code:	Package Shape:
PLASTIC/EPOXY	FBGA	BGA484,22X22,32	SQUARE
Package Style:	Peak Reflow Temperature (Cel):	Programmable Logic Type:	Qualification Status:
GRID ARRAY, FINE PITCH	NOT SPECIFIED	FIELD PROGRAMMABLE GATE ARRAY	Not Qualified
Seated Height-Max:	Subcategory:	Supply Voltage-Max:	Supply Voltage-Min:
2.05 mm	Field Programmable Gate Arrays	1.25 V	1.15 V
Supply Voltage-Nom:	Surface Mount:	Technology:	Terminal Finish:
1.2 V	YES	CMOS	Tin/Silver/Copper (Sn/Ag/Cu)
Terminal Form:	Terminal Pitch:	Terminal Position:	Time@Peak Reflow Temperature-Max (s):
BALL	0.8 mm	BOTTOM	NOT SPECIFIED
Width:			
19 mm			

5SGXMA7K2F40C2N	168	BGA	20+	ALTERA
5SGXMA7K3F40C2N	168	FBGA1156	20+	ALTERA
5SGXMA9K3H40C2N	103	BGA	20+	ALTERA
5SGXMA9K3H40I3N	156	BGA	20+	ALTERA
5SGXMA9K3H40I4N	142	BGA	20+	ALTERA
EP1S20F484C6	1000	BGA	20+	XILINX
EP1S20F484C6N	1000	BGA	20+	XILINX
EP1S20F484I6	100	BGA	20+	ALTERA
EP1S20F484I6N	187	BGA484	20+	ALTERA
EP1S20F672I7	1500	BGA	20+	ALTERA
EP1S20F672I7N	150	FBGA676	20+	ALTERA
EP1S20F780I6	72	BGA	20+	ALTERA
EP1S25F1020C6	300	FCBGA	20+	ALTERA
EP1S25F1020I6	38	BGA	20+	ALTERA
EP1S25F1020I6N	120	FBGA	20+	ALTERA
EP1S25F672C6	144	BGA	20+	ALTERA
EP1S25F672C6N	160	FCBGA	20+	ALTERA
EP1S25F672C7	500	BGA	20+	ALTERA
EP1S25F672C7N	200	FBGA	20+	ALTERA
EP1S25F672I7	500	BGA	20+	ALTERA
EP1S25F780C7N	248	BGA1136	20+	ALTERA
EP1S25F780I6	42	BGA	20+	ALTERA
EP1S30F1020I6	168	BGA	20+	ALTERA
EP1S30F1020I6N	50	BGA	20+	ALTERA
EP1S30F780I6	172	BGA	20+	ALTERA
EP1S30F780I6N	195	FBGA676	20+	ALTERA
EP1S40B956I6	228	BGA	20+	ALTERA
EP1S40F1020I6	480	BGA	20+	ALTERA
EP1S40F780I6	240	BGA	20+	ALTERA
EP1S60B956I7	332	BGA	20+	ALTERA
EP1S60F1020C6N	56	FBGA1926	20+	ALTERA
EP1S60F1020C7N	20	FBGA1157	20+	ALTERA
EP1S80F1020C5N	143	BGA1759	20+	ALTERA
EP1S80F1020I6N	453	FCBGA1156	20+	ALTERA
EP1SGX25DF672C7N	20	BGA	20+	ALTERA
EP1SGX40DF1020C6N	386	BGA	20+	ALTERA
EP1SGX40GF1020I6	5	BGA	20+	ALTERA

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the "PLLs & Clock Networks" section). Figure 2–49 illustrates the signal paths through the I/O block.

Figure 2–49. Signal Path through the I/O Block
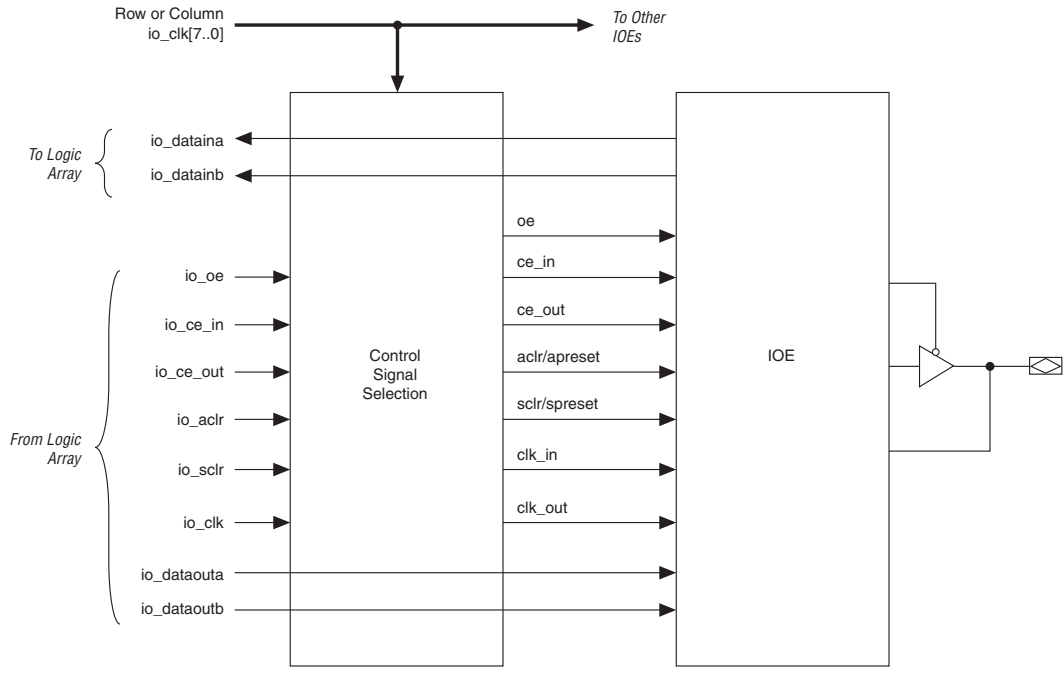
Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.