The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figures 2–37 through 2–39.

The following restrictions for the input clock pins apply:

- CLK0 pin -> inclk[0] of CLKCTRL
- CLK1 pin -> inclk[1] of CLKCTRL
- CLK2 pin -> inclk[0] of CLKCTRL
- CLK3 pin -> inclk[1] of CLKCTRL

In general, even CLK numbers connect to the inclk[0] port of CLKCTRL, and odd CLK numbers connect to the inclk[1] port of CLKCTRL.

Failure to comply with these restrictions will result in a no-fit error.

Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread-spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

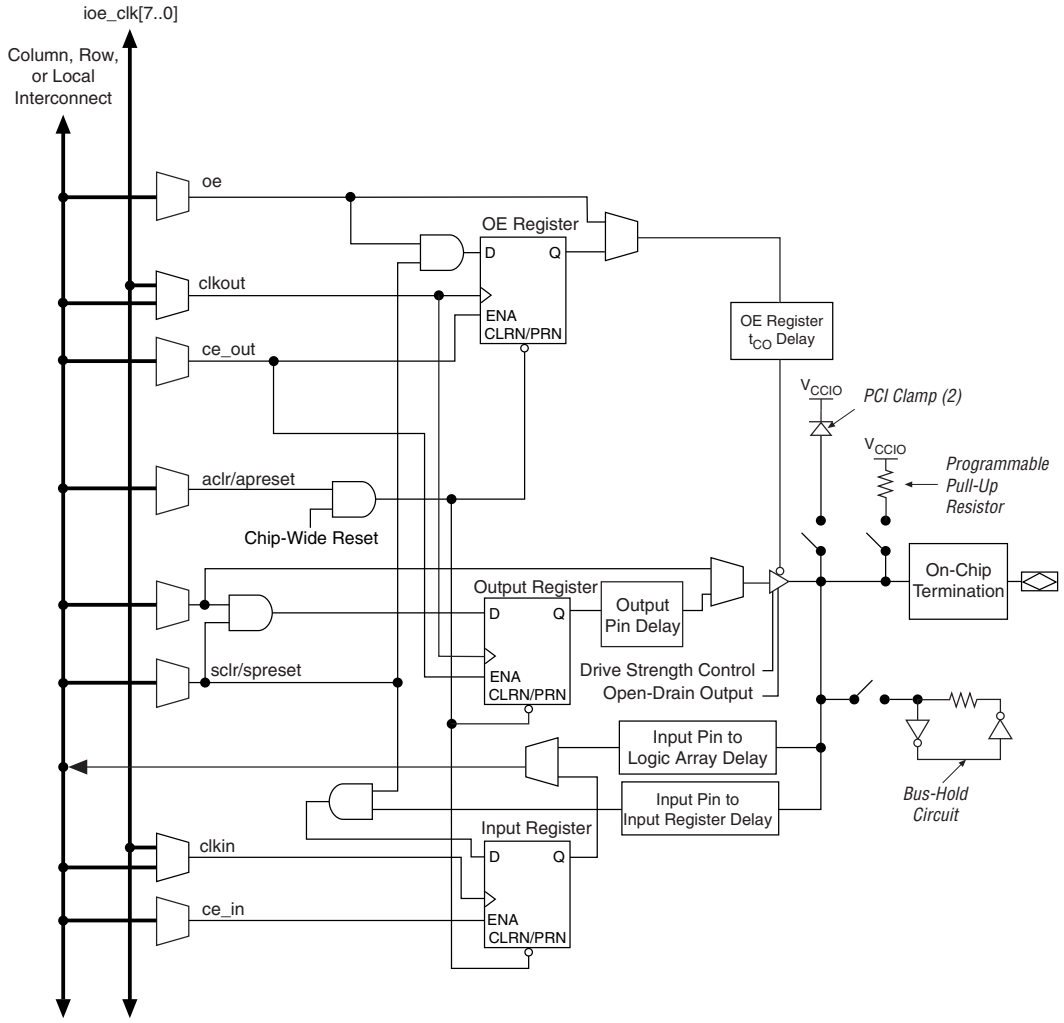
芯片详细信息

Manufacturer Part Number: EP3C80U484C8N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: 19 X 19 MM, 2.20 MM HEIGHT, 0.80 MM PITCH, LEAD FREE, UFBGA-484	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.29	Clock Frequency-Max: 472.5 MHz	JESD-30 Code: R-PBGA-B484
JESD-609 Code: e1	Length: 19 mm	Moisture Sensitivity Level: 3	Number of CLBs: 81264
Number of Inputs: 295	Number of Logic Cells: 81264	Number of Outputs: 295	Number of Terminals: 484
Operating Temperature-Max: 85 °C	Organization: 81264 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: FBGA
Package Equivalence Code: BGA484,22X22,32	Package Shape: RECTANGULAR	Package Style: GRID ARRAY, FINE PITCH	Peak Reflow Temperature (Cel): 260
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.2 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V	Surface Mount: YES
Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: TIN SILVER COPPER	Terminal Form: BALL
Terminal Pitch: 0.8 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 40	Width: 19 mm

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Cyclone III	☐
系列:	Cyclone III EP3C80	☐
逻辑元件数量:	81264 LE	☐
自适应逻辑模块 - ALM:	-	☐
嵌入式内存:	2.68 Mbit	☐
输入/输出端数量:	295 I/O	☐
工作电源电压:	1.15 V to 1.25 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	BGA-484	☐
封装:	Tray	☐
商标:	Intel / Altera	
最大工作频率:	315 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	5079 LAB	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	84	
子类别:	Programmable Logic ICs	
总内存:	2810880 bit	
商标名:	Cyclone III	
零件号别名:	966959	
单位重量:	7.100 g	

Figure 2–51 shows the IOE in bidirectional configuration.

Figure 2–51. Stratix II IOE in Bidirectional I/O Configuration *Note (1)*



Notes to Figure 2–51:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The optional PCI clamp is only available on column I/O pins.

The Stratix II device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create the zero hold time for these transfers. Table 2–13 shows the programmable delays for Stratix II devices.

Table 2–13. Stratix II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

The IOE registers in Stratix II devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Stratix II devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.