Accessing Configuration Registers through the JTAG Interface

JTAG access to the Spartan-6 FPGA configuration logic is provided through the JTAG CFG_IN and CFG_OUT registers. The CFG_IN and CFG_OUT registers are not configuration registers, rather they are JTAG registers like BYPASS and BOUNDARY_SCAN. Data shifted into the CFG_IN register goes to the configuration packet processor, where it is processed in the same way commands from the SelectMAP interface are processed.

Readback commands are written to the configuration logic by going through the CFG_IN register; configuration memory is read through the CFG_OUT register. The JTAG state transitions for accessing the CFG_IN and CFG_OUT registers are described in Table 6-4.

Table 6-4: **Shifting in the JTAG CFG_IN and CFG_OUT Instructions**

Step	Description	Set and Hold		# of Clocks (TCK)
		TDI	TMS	
1	Clock five *1*s on TMS to bring the device to the TLR state	X	1	5
2	Move into the RTI state	X	0	1
3	Move into the Select-IR state	X	1	2
4	Move into the Shift-IR state	X	0	2
5	Shift the first five bits of the CFG_IN or CFG_OUT instruction, LSB first	000101 (CFG_IN) 000100 (CFG_OUT)	0	5
6	Shift the MSB of the CFG_IN or CFG_OUT instruction while exiting SHIFT-IR	0	1	1
7	Move into the SELECT-DR state	X	1	2
8	Move into the SHIFT-DR state	X	0	2
9	Shift data into the CFG_IN register or out of the CFG_OUT register while in SHIFT_DR, MSB first	X	0	X
10	Shift the LSB while exiting SHIFT-DR	X	1	1
11	Reset the TAP by clocking five *1*s on TMS	X	1	5

Configuration Register Read Procedure (JTAG)

The simplest read operation targets a configuration register such as the COR0 or STAT register. Any configuration register with read access can be read through the JTAG interface, although not all registers offer read access. The procedure for reading the STAT register through the JTAG interface follows:

1. Reset the TAP controller.
2. Shift the CFG_IN instruction into the JTAG Instruction Register through the Shift-IR state. The LSB of the CFG_IN instruction is shifted first; the MSB is shifted while moving the TAP controller out of the SHIFT-IR state.
3. Shift packet write commands into the CFG_IN register through the Shift-DR state:
   a. Write the synchronization word to the device.
   b. Write the *read STAT register* packet header to the device.
   c. Write two dummy words to the device to flush the packet buffer.

The MSB of all configuration packets sent through the CFG_IN register must be sent first. The LSB is shifted while moving the TAP controller out of the SHIFT-DR state.

4. Shift the CFG_OUT instruction into the JTAG Instruction Register through the Shift-IR state. The LSB of the CFG_OUT instruction is shifted first; the MSB is shifted while moving the TAP controller out of the SHIFT-IR state.
5. Shift 32 bits out of the Status register through the Shift-DR state.
6. Reset the TAP controller.

Table 6-5: **Status Register Readback Command Sequence (JTAG)**

Step	Description	Set and Hold		# of Clocks (TCK)
		TDI	TMS	
1	Clock five 1s on TMS to bring the device to the TLR state.	X	1	5
	Move into the RTI state.	X	0	1
	Move into the Select-IR state.	X	1	2
	Move into the Shift-IR state.	X	0	2
2	Shift the first five bits of the CFG_IN instruction, LSB first.	00101 (CFG_IN)	0	5
	Shift the MSB of the CFG_IN instruction while exiting SHIFT-IR.	0	1	1
	Move into the SELECT-DR state.	X	1	2
	Move into the SHIFT-DR state.	X	0	2
3	Shift configuration packets into the CFG_IN data register, MSB first.	a: 0xAA99 a: 0x5566 b: 0x2901 c: 0x2000 c: 0x2000 d: 0x2000 d: 0x2000	0	111
	Shift the LSB of the last configuration packet while exiting SHIFT-DR.	0	1	1
	Move into the SELECT-IR state.	X	1	3
	Move into the SHIFT-IR state.	X	0	2
4	Shift the first five bits of the CFG_OUT instruction, LSB first.	00100 (CFG_OUT)	0	5
	Shift the MSB of the CFG_OUT instruction while exiting Shift-IR.	0	1	1
	Move into the SELECT-DR state.	X	1	2
	Move into the SHIFT-DR state.	X	0	2

XC2S600E-2FG456I	2001+	原厂原封	2315
XC2S600E-2FG456C	2001+	BGA	2315
XC2S600E-2FG456	2001+	BGA	2315
XC2S600E-1FG676I	2001+	BGA	2315
XC2S600E-1FG676C	2001+	BGA	2315
XC2S600E-1FG456I	2001+	原厂原封	2315
XC2S600E-1FG456C	2001+	原厂原封	2315
XC2S600E 6FGG456C	2001+	FCBGA	2315
XC2S600E	2001+	BGA	2315
XC2S600-6FG456I	2001+	BGA	2315
XC2S600-6FG456C	2001+	BGA	2315
XC2S600-4FG456C	2001+	BGA	2315
XC2S6000EFG676AGT-7C	2001+	BGA	2315
XC2S600 6FGG456C	2001+	FCBGA	2315
XC2S50E-TQG144AGT	2001+	SOP	2315
XC2S50ETM	2001+	N A	2315
XC2S50E PQ208	2001+	QFP	2315
XC2S550E6FT256C	2001+	BGA	2315
XC2S512FG324	2001+	BGA	2315
XC2S512-2FT256	2001+	BGA	2315
XC2S512-1FGG324	2001+	BGA	2315
XC2S512-10PQG208C	2001+	QFP208	2315
XC2S512-10FT256	2001+	BGA	2315
XC2S512-10FGG324C	2001+	BGA	2315
XC2S510-5FG256C	2001+	BGA	2315
XC2S50XLPQ208-5C	2001+	QFP	2315
XC2S50TQG144AMS	2001+	QFP144	2315
XC2S50-TQG144	2001+	QFP	2315
XC2S50TQG144	2001+	QFP	2315
XC2S50TQC144AMS	2001+	QFP144	2315
XC2S50TQ144C5	2001+	QFP	2315
XC2S50-TQ144AMS	2001+	QFP-144	2315
XC2S50TQ144AMS	2001+	QFP	2315
XC2S50TQ144-5C	2001+	QFP	2315
XC2S50TQ144	2001+	QFP	2315
XC2S50TMPQ208-5I	2001+	QFP	2315
XC2S50TMPQ208-5C	2001+	QFP	2315
XC2S50TM-6TQ144CAMS	2001+	QFP	2315
XC2S50TM-5C	2001+	QFP144	2315
XC2S50TM	2001+	TQFP144	2315
XC2S50-PQG208AMS	2001+	QFP144	2315

After the configuration logic receives the IPROG command, the FPGA resets everything except the dedicated reconfiguration logic, and the INIT_B and DONE pins go Low. After the FPGA clears all configuration memory, INIT_B goes High again. Then the value in GENERAL1,2 is used for the bitstream starting address.

IPROG does not reset the strike count. MultiBoot applications that use IPROG through ICAP_SPARTAN6 should pulse PROGRAM_B or implement a power cycle after a configuration error that increments the strike count. Otherwise, verify that external memory is properly updated to avoid configuration errors that would increment the strike count.

Status Register for Fallback and IPROG Reconfiguration

Spartan-6 devices contain a BOOTSTS that stores configuration history. At EOS or an error condition, Status_0 is updated with the current status. If fallback or MultiBoot occurs, Status_1 is updated at EOS or an error condition. The Valid_0 bit indicates if the rest of Status_0 is valid or not. The BOOTSTS register is written either at an End Of Startup (EOS) event or a fallback event. The EOS event happens after the first configuration attempt. A successful MultiBoot operation via the IPROG command does not result in the BOOTSTS register being updated. See Boot History Status Register (BOOTSTS), page 110.

Table 7-2 through Table 7-4 show the BOOTSTS values in some common situations.

Table 7-2: **Status after First Bitstream Configuration without Error**

	CRC_ERROR	ID_ERROR	WTO_ERROR	IPROG	FALLBACK	VALID
Status_1	0	0	0	0	0	0
Status_0	0	0	0	0	0	1

Table 7-3: **First Configuration followed by IPROG**

	CRC_ERROR	ID_ERROR	WTO_ERROR	IPROG	FALLBACK	VALID
Status_1	0	0	0	0	0	1
Status_0	0	0	0	1	0	1

Table 7-4: **IPROG Embedded in First Bitstream, Second Bitstream CRC Error, and Fallback Successfully**

	CRC_ERROR(1)	ID_ERROR	WTO_ERROR	IPROG	FALLBACK	VALID
Status_1(2)	0	0	0	1	1	1
Status_0(3)	1	0	0	1	0	1

Notes:

1. CRC_Error only registers CRC errors detected during initial configuration. CRC_Error is not updated if CRC errors are found from the Readback CRC (POST_CRC) function.
2. Status_1 shows a fallback bitstream was loaded successfully. The IPROG bit was also set in this case, because the fallback bitstream contains an IPROG command. Although the IPROG command is ignored during fallback, the status still records this occurrence.
3. Status_0 shows IPROG was attempted, and a CRC_ERROR was detected for that bitstream.

XC2S50-PQG208	2001+	BGA	2315
XC2S50PQG208	2001+	LQFP208	2315
XC2S50-PQ208AMS-5C	2001+	QFP	2315
XC2S50-PQ208AMS	2001+	BGA	2315
XC2S50PQ208AMS	2001+	QFP208	2315
XC2S50PQ208AM	2001+	QFP	2315
XC2S50-PQ208AFP	2001+	QFP	2315
XC2S50PQ208AFP	2001+	QFP	2315
XC2S50-PQ2085C	2001+	TQFP	2315
XC2S50PQ208-5C	2001+	QFP	2315
XC2S50-PQ208-4C	2001+	QFP	2315
XC2S50-PQ208	2001+	qfp208	2315
XC2S50PQ208	2001+	QFP	2315
XC2S50PQ 208AFP	2001+	BGA	2315
XC2S50FT256	2001+	BGA	2315
XC2S50FGG256AMS	2001+	BGA	2315
XC2S50FGG256	2001+	BGA	2315
XC2S50-FG256CAMS	2001+	BGA	2315
XC2S50FG256AMS0841	2001+	BGA	2315
XC2S50-FG256AMS	2001+	BGA	2315
XC2S50FG256AMS	2001+	BGA	2315
XC2S50FG256-6C	2001+	BGA-256D	2315
XC2S50FG256-5I	2001+	BGA	2315
XC2S50-FG256-5C	2001+	BGA	2315
XC2S50FG256-5C	2001+	BGA	2315
XC2S50-FG256	2001+	BGA256	2315
XC2S50FG256	2001+	QFP	2315
XC2S50E-TQG144AGT	2001+	TQFP144	2315
XC2S50E-TQG144-6I	2001+	TQFP144	2315
XC2S50E-TQG144-6C	2001+	TQFP144	2315
XC2S50E-TQG144	2001+	QFP	2315
XC2S50ETQ144AMT	2001+	QFP	2315
XC2S50E-TQ144AGT	2001+	QFP	2315
XC2S50ETQ144AGT	2001+	BGA	2315
XC2S50ETQ144-6I	2001+	QFP	2315
XC2S50ETQ144-6C	2001+	QFP	2315
XC2S50E-TQ144-6C	2001+	QFP	2315
XC2S50ETQ144	2001+	BGA	2315
XC2S50ETM-6C	2001+	QFP144	2315
XC2S50E-PQG208	2001+	QFP	2315
XC2S50E-PQ208AGT	2001+	QFP	2315