Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
K17	DDR3_CAS_B	SSTL15	115	CAS_B
E20	DDR3_RAS_B	SSTL15	110	RAS_B
K19	DDR3_CKE0	SSTL15	73	CKE0
J18	DDR3_CKE1	SSTL15	74	CKE1
G18	DDR3_CLK0_N	DIFF_SSTL15	103	CK0_N
H19	DDR3_CLK0_P	DIFF_SSTL15	101	CK0_P
F19	DDR3_CLK1_N	DIFF_SSTL15	104	CK1_N
G19	DDR3_CLK1_P	DIFF_SSTL15	102	CK1_P

The VC707 DDR3 SODIMM interface adheres to the constraints guidelines in the DDR3 *Design Guidelines* section of *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 4]. The VC707 DDR3 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are available in UG586 and *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 5]. For more details on the DDR3 SODIMM, see the Micron Semiconductor MT8JTF12864HZ-1G6G1 data sheet [Ref 17].

Linear BPI Flash Memory

[Figure 1-2, callout 3]

The Linear BPI Flash memory located at U3 provides 128 MB of nonvolatile storage that can be used for configuration or software storage. The data, address, and control signals are connected to the FPGA. The BPI Flash memory device is packaged in a 64-pin BGA.

- Part number: PC28F00AG18FE (Micron)
- Supply voltage: 1.8V
- Datapath width: 16 bits (26 address lines and 7 control signals)
- Data rate: Up to 80 MHz

The Linear BPI Flash memory can synchronously configure the FPGA in Master BPI mode at the 80 MHz data rate supported by the PC28F00AG18FE flash memory. The fastest configuration method uses the external 80 MHz oscillator connected to the FPGA's EMCCLK pin.

Multiple bitstreams can be stored in the Linear BPI Flash. The two most significant address bits (A25, A24) of the flash memory are connected to DIP switch SW11 positions 1 and 2 respectively, and to the RS1 and RS0 pins of the FPGA. By placing valid XC7VX485T bitstreams at four different offset addresses in the flash memory, 1 of the 4 bitstreams can be selected to configure the FPGA by appropriately setting the DIP switch SW11. The connections between the BPI Flash memory and the FPGA are listed in Table 1-5.

System Clock (SYSCLK_P and SYSCLK_N)

[Figure 1-2, callout 7]

The VC707 board has a LVDS 200 MHz oscillator (U51) soldered onto the back side of the board and wired to an FPGA MRCC clock input on bank 38. This 200 MHz signal pair is named SYSCLK_P and SYSCLK_N, which are connected to FPGA U1 pins E19 and E18 respectively.

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- PPM frequency tolerance: 50 ppm
- Differential Output

For more details, see the SiTime SiT9102 data sheet [Ref 19]. The system clock circuit is shown in Figure 1-9.

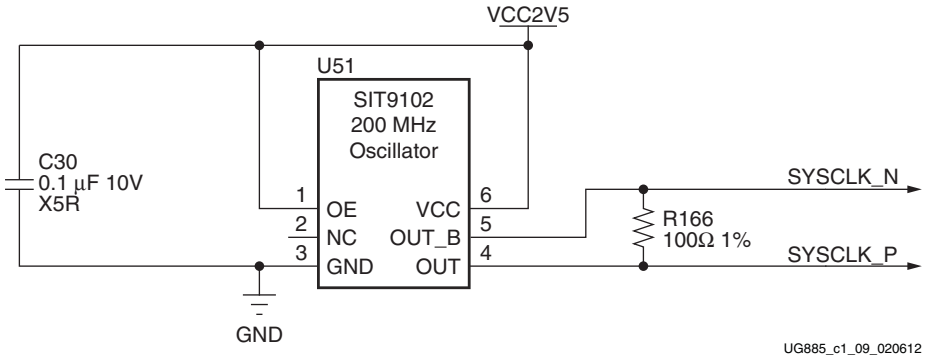

Figure 1-9: **System Clock Source**

Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N)

[Figure 1-2, callout 8]

The VC707 board has a programmable low-jitter 3.3V differential oscillator (U34) connected to the FPGA MRCC inputs of bank 14. This USER_CLOCK_P and USER_CLOCK_N clock signal pair are connected to FPGA U1 pins AK34 and AL34 respectively. On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I^2C interface. Power cycling the VC707 board reverts the user clock to its default frequency of 156.250 MHz.

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz - 810 MHz)
- Differential Output

SGMII GTX Transceiver Clock Generation

[Figure 1-2, callout 16]

An Integrated Circuit Systems ICS844021I chip (U2) generates a high-quality, low-jitter, 125 MHz LVDS clock from a 25 MHz crystal (X3). This clock is sent to FPGA U1, Bank 113 GTX transceiver (clock pins AH8 (P) and AH7 (N)) driving the SGMII interface. Series AC coupling capacitors are present to allow the clock input of the FPGA to set the common mode voltage. Figure 1-17 shows the Ethernet SGMII clock source.

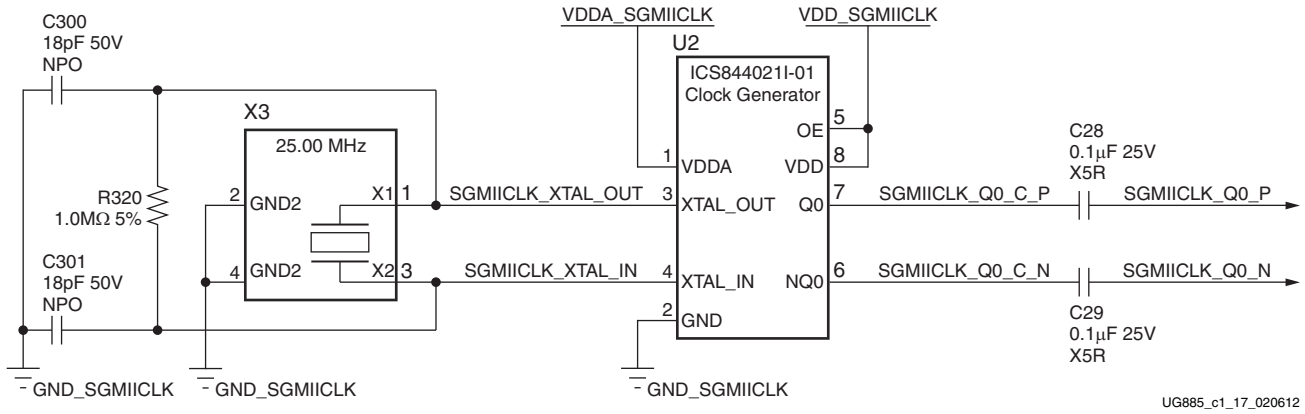

Figure 1-17: **Ethernet 125 MHz SGMII GTX Clock**

References

Details about the tri-mode Ethernet MAC core are provided in *LogiCORE IP Tri-Mode Ethernet MAC Product Guide for Vivado Design Suite* (PG051) [Ref 9] and in the *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide* (UG138) [Ref 13].

The product brief for the Marvell 88E1111 Alaska Gigabit Ethernet Transceiver can be found at the Marvell website [Ref 21].

The data sheet can be obtained under NDA with Marvell. Contact information is at the Marvell website [Ref 21].

For more information about the ICS844021 device, go to the Integrated Device Technology website [Ref 22] and search for part number **ICS844021**.

USB-to-UART Bridge

[Figure 1-2, callout 17]

The VC707 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U44) which allows a connection to a host computer with a USB port. The USB cable is supplied in the VC707 Evaluation Kit (Type-A end to host computer, Type mini-B end to VC707 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VC707 board.

Xilinx UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using four signal pins: Transmit (TX), Receive (RX), Request to Send (RTS), and Clear to Send (CTS).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm) that runs on the host computer. The VCP device

芯片详细信息

Manufacturer Part Number: XC2V8000-6FF1152I	Pbfree Code: No	Rohs Code: No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: 35 X 35 MM, 1 MM PITCH, MS-034AAR-1, FLIP CHIP, FBGA-1152	Pin Count: 1152
Reach Compliance Code: not_compliant	HTS Code: 8542.39.00.01	Manufacturer: Xilinx	Risk Rank: 5.85
Clock Frequency-Max: 820 MHz	Combinatorial Delay of a CLB-Max: 0.35 ns	JESD-30 Code: S-PBGA-B1152	JESD-609 Code: e0
Length: 35 mm	Moisture Sensitivity Level: 4	Number of CLBs: 11648	Number of Equivalent Gates: 8000000
Number of Inputs: 824	Number of Logic Cells: 104832	Number of Outputs: 824	Number of Terminals: 1152
Organization: 11648 CLBS, 8000000 GATES	Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA1152,34X34,40
Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 225	Power Supplies: 1.5,1.5/3.3,3.3 V
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.4 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V	Surface Mount: YES
Technology: CMOS	Terminal Finish: Tin/Lead (Sn63Pb37)	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 35 mm	

XC2S400E-7FTG256I	2001+	BGA	2315
XC2S400E-7FTG256C	2001+	BGA	2315
XC2S400E-7FT256I	2001+	BGA	2315
XC2S400E-7FT256C	2001+	BGA	2315
XC2S400E-7FGG676I	2001+	BGA	2315
XC2S400E-7FGG676C	2001+	BGA	2315
XC2S400E-7FGG456I	2001+	BGA	2315
XC2S400E-7FGG456C	2001+	BGA	2315
XC2S400E-7FG676I	2001+	BGA	2315
XC2S400E-7FG676C	2001+	BGA	2315
XC2S400E-7FG676	2001+	BGA	2315
XC2S400E-7FG456I	2001+	QFP	2315
XC2S400E-7FG456C	2001+	BGA-456	2315
XC2S400E-7FG456	2001+	BGA	2315
XC2S400E-6TQG144I	2001+	BGA	2315
XC2S400E-6TQG144C	2001+	BGA	2315
XC2S400E-6TQ144I	2001+	BGA	2315
XC2S400E-6TQ144C	2001+	BGA	2315
XC2S400E-6PQG208I	2001+	BGA	2315
XC2S400E-6PQG208C	2001+	BGA	2315
XC2S400E-6PQ208I	2001+	BGA	2315
XC2S400E-6PQ208C	2001+	BGA	2315
XC2S400E-6FTG256I/7C	2001+	BGA	2315
XC2S400E-6FTG256I	2001+	BGA256	2315
XC2S400E-6FTG256C	2001+	BGA256	2315
XC2S400E-6FTG256C	2001+	BGA256	2315
XC2S400E-6FT256I	2001+	BGA	2315
XC2S400E-6FT256C	2001+	BGA	2315
XC2S400E6FT256C	2001+	BGA	2315
XC2S400E-6FT256	2001+	BGA	2315
XC2S400E-6FGG676I/7C	2001+	BGA	2315
XC2S400E-6FGG676I	2001+	BGA	2315
XC2S400E-6FGG676C	2001+	BGA	2315
XC2S400E-6FGG456I	2001+	BGA456	2315
XC2S400E-6FGG456C	2001+	BGA	2315
XC2S400E-6FGF676I	2001+	13	2315
XC2S400E-6FG676I	2001+	BGA	2315
XC2S400E-6FG676CN	2001+	BGA	2315
XC2S400E-6FG676C	2001+	BGA	2315
XC2S400E6FG676C	2001+	bga	2315
XC2S400E-6FG676	2001+	BGA	2315