DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

Table 28: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND			–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND			–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND			–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	
	Voltage applied to all Dedicated pins relative to GND(3)		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V

Table 30: **Power Voltage Ramp Time Requirements**

Symbol	Description	Device	Package	Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	All	All	No limit(4)	–	N/A
T_{CCINT}	V_{CCINT} ramp time, only if V_{CCINT} is last in three-rail power-on sequence	All	All	No limit	No limit(5)	N/A

Notes:

1. If a limit exists, this specification is based on characterization.
2. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
3. For information on power-on current needs, see Power-On Behavior, page 54
4. For mask revisions earlier than revision E (see Mask and Fab Revisions, page 58), T_{CCO} min is limited to 2.0 ms for the XC3S200 and XC3S400 devices in QFP packages, and limited to 0.6 ms for the XC3S200, XC3S400, XC3S1500, and XC3S4000 devices in the FT and FG packages.
5. For earlier device versions with the FQ fabrication/process code (see Mask and Fab Revisions, page 58), T_{CCINT} max is limited to 500 µs.

Table 31: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include data stored in CMOS configuration latches.
2. The level of the V_{CCO} supply has no effect on data retention.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage indicated in Table 29 in order to clear out the device configuration content.

Table 32: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	25	85	°C
		Industrial	–40	25	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.140	–	3.465	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX}(2)	Voltage variance on VCCAUX when using a DCM		–	–	10	mV/ms
V_{IN}(3)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(4)(6)	V_{CCO} = 3.3V, IO	–0.3	–	3.75	V
		V_{CCO} = 3.3V, IO_Lxxy(7)	–0.3	–	3.75	V
		$V_{CCO} \le$ 2.5V, IO	–0.3	–	V_{CCO} + 0.3(4)	V
		$V_{CCO} \le$ 2.5V, IO_Lxxy(7)	–0.3	–	V_{CCO} + 0.3(4)	V
	Voltage applied to all Dedicated pins relative to GND(5)		–0.3	–	V_{CCAUX} + 0.3(5)	V

Notes:

1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 35, and that specific to the differential standards is given in Table 37.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Input voltages outside the recommended range are permissible provided that the I_{IK} input diode clamp diode rating is met. Refer to Table 28.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 28.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
6. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
7. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3), IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

芯片详细信息

Manufacturer Part Number: XC2V8000-5FFG1152C	Pbfree Code: Yes	Rohs Code: Yes	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: 35 X 35 MM, 1 MM PITCH, MS-034AAR-1, FLIP CHIP, FBGA-1152	Pin Count: 1152
Reach Compliance Code: not_compliant	ECCN Code: 3A001.A.7.A	HTS Code: 8542.39.00.01	Manufacturer: Xilinx
Risk Rank: 5.8	Clock Frequency-Max: 750 MHz	Combinatorial Delay of a CLB-Max: 0.39 ns	JESD-30 Code: S-PBGA-B1152
JESD-609 Code: e1	Length: 35 mm	Moisture Sensitivity Level: 4	Number of CLBs: 11648
Number of Equivalent Gates: 8000000	Number of Terminals: 1152	Operating Temperature-Max: 85 °C	Organization: 11648 CLBS, 8000000 GATES
Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 245	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.4 mm
Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V	Surface Mount: YES
Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: Tin/Silver/Copper (Sn95.5Ag4.0Cu0.5)	Terminal Form: BALL
Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 35 mm

XC2V30-4FFG896C	2001+	BGA	2315
XC2V30-4FF896C	2001+	BGA	2315
XC2V300-FG676AGT	2001+	BGA676	2315
XC2V300-5FG676C	2001+	BGA676	2315
XC2V300-4FG676C	2001+	BGA	2315
XC2V300-4BF957I	2001+	BGA957	2315
XC2V3000TM-5CFG676	2001+	BGA	2315
XC2V3000TM	2001+	N A	2315
XC2V3000FGG676AGT	2001+	BGA	2315
XC2V3000FG728C5	2001+	BGA	2315
XC2V3000FG676AGT-4	2001+	BGA	2315
XC2V3000-FG676AGT	2001+	BGA	2315
XC2V3000FG676AGT	2001+	BGA	2315
XC2V3000FG676AF	2001+	BGA	2315
XC2V3000-FG676-4C	2001+	BGA	2315
XC2V3000FG676-4C	2001+	BGA	2315
XC2V3000-FG676	2001+	BGA	2315
XC2V3000FG676	2001+	BGA676	2315
XC2V3000-FFF1152C	2001+	BGA1152	2315
XC2V3000FF957	2001+	BGA	2315
XC2V3000FF1152BGT	2001+	BGA	2315
XC2V3000-FF1152AGT	2001+	BGA	2315
XC2V3000FF1152AGT	2001+	BGA	2315
XC2V3000-FF1152AF	2001+	BGA	2315
XC2V3000FF1152-4C	2001+	BGA	2315
XC2V3000-FF1152	2001+	BGA	2315
XC2V3000FF1152	2001+	BGA	2315
XC2V3000FF1150	2001+	BGA	2315
XC2V3000BG957	2001+	BGA	2315
XC2V3000-BG728C	2001+	BGA	2315
XC2V3000-BG728	2001+	BGA	2315
XC2V3000BG728	2001+	BGA	2315
XC2V3000-BF957AGT-4C	2001+	BGA	2315
XC2V3000BF957AGT0309	2001+	BGA	2315
XC2V3000-BF957AGT	2001+	BGA957	2315
XC2V3000BF957AGT	2001+	BGA957	2315
XC2V3000-BF957AFT	2001+	BGA	2315
XC2V3000-BF957AFT	2001+	BGA	2315
XC2V3000BF957-5C	2001+	BGA	2315
XC2V3000-BF957	2001+	PBGA	2315
XC2V3000-7FGG676C	2001+	BGA	2315