TX Gearbox

Overview

Some high-speed data rate protocols use 64B/66B encoding to reduce the overhead of 8B/10B encoding while retaining the benefits of an encoding scheme. The TX Gearbox provides support for 64B/66B and 64B/67B header and payload combining. The Interlaken interface protocol specification uses the 64B/67B encoding scheme. Refer to the Interlaken specification for further information. The TX Gearbox only supports 2-byte and 4-byte interfaces. A 1-byte interface is not supported.

Scrambling of the data is done in the FPGA logic. The RocketIO™ GTX Transceiver Wizard has example code for the scrambler.

Ports and Attributes

Table 6-6 defines the TX Gearbox ports.

Table 6-6: **TX Gearbox Ports**

Port	Direction	Clock Domain	Description
TXGEARBOXREADY0 TXGEARBOXREADY1	Out	TXUSRCLK2	Output indicating how data is applied to TX Gearbox. `0`: No data can be applied `1`: Data must be applied Use with attributes GEARBOX_ENCDEC_0 and GEARBOX_ENCDEC_1.
TXHEADER0[2:0] TXHEADER1[2:0]	In	TXUSRCLK2	Input for header bits. Bit[2]: Indicates data inverted for 64B/67B encoding Bit[1:0]: The encoding for these bits is: `01`: Data header `10`: Control header
TXSEQUENCE0[6:0] TXSEQUENCE1[6:0]	In	TXUSRCLK2	Input from 7-bit/6-bit counter in FPGA logic to the TX Gearbox. Time to data for 64B/67B and 64B/66B.
TXSTARTSEQ0 TXSTARTSEQ1	In	TXUSRCLK2	Input to TX Gearbox indicating the first character in the data sequence for 64B/67B and 64B/66B encoding.

Table 6-7 defines the TX Gearbox attributes.

Table 6-7: **TX Gearbox Attributes**

Attribute	Type	Description
GEARBOX_ENDEC_0[2:0] GEARBOX_ENDEC_1[2:0]	3-bit Binary	Indicates TX Gearbox modes: Bit [2]: Always set to 0 to enable the Gearbox decoder Bit [1]: The encoding for this bit is: 0: Use external sequence counter and apply inputs to TXSEQUENCE 1: Use internal sequence counter, gate input header, and data with output TXGEARBOXREADY0 and TXGEARBOXREADY1 Bit [0]: The encoding for this bit is: 0: 64B/67B Gearbox mode for Interlaken 1: 64B/66B Gearbox
TXGEARBOX_USE_0 TXGEARBOX_USE_1	Boolean	When TXGEARBOX_USE = TRUE, TX Gearbox is enabled. The TX Gearbox only supports 2-byte and 4-byte logic interfaces. When using the internal TX Gearbox, a 1-byte logic interface is not supported. A 1-byte logic interface can be implemented by using an external Gearbox in the FPGA logic. INTDATAWIDTH must be 0 (16-bit internal data width mode) when the TX Gearbox is enabled.

Description

Enabling the TX Gearbox

To enable the TX Gearbox for the GTX transceiver 0, set the attribute TXGEARBOX_USE_0 to TRUE. To enable the TX Gearbox for the GTX transceiver 1, set the attribute TXGEARBOX_USE_1 to TRUE.

Bit 2 of the GEARBOX_ENDEC attribute must be set to 0 to enable the Gearbox decoder. The decoder controls the GTX transceiver's TX Gearbox and RX Gearbox. The GTX transceiver's TX Gearbox and RX Gearbox use the same mode.

TX Gearbox Bit and Byte Ordering

Figure 6-11 shows an example of the first five cycles of data entering and data exiting the TX Gearbox for 64B/66B encoding when using a two-byte logic interface. The input consists of a 2-bit header and 16 bits of data. On the first cycle, the header and 14 bits of data exit the TX Gearbox. On the second cycle, the remaining two data bits from the previous cycle's TXDATA input along with 14 data bits from the current TXDATA input exit the TX Gearbox. This continues for the third and fourth cycle. On the fifth cycle, the output of the TX Gearbox contains two remaining data bits from the first 66-bit block, the header of the second 66-bit block, and 12 data bits from the second 66-bit block. As shown in Figure 6-11, the header bits are serialized first followed by the data bits.

TX PRBS Generator

Overview

Pseudo-random bit sequences (PRBS) are commonly used to test the signal integrity of high-speed links. These sequences appear random but have specific properties that can be used to measure the quality of a link.

The GTX PRBS block can generate several industry-standard PRBS patterns. Table 6-13 lists the available PRBS patterns and their typical uses.

Table 6-13: **Pseudo-Random Bit Sequences**

Name	Polynomial	Length of Sequence (bits)	Consecutive Zeros	Typical Use
PRBS-7	$1 + X^6 + X^7$ (inverted)	$2^7 - 1$	7	Used to test channels with 8B/10B.
PRBS-23	$1 + X^{18} + X^{23}$ (inverted)	$2^{23} - 1$	23	ITU-T Recommendation O.150, Section 5.6. One of the recommended test patterns in the SONET specification.
PRBS-31	$1 + X^{28} + X^{31}$ (inverted)	$2^{31} - 1$	31	ITU-T Recommendation O.150, Section 5.8. A recommended PRBS test pattern for 10 Gigabit Ethernet. See IEEE 802.3ae-2002.

Ports and Attributes

Table 6-14 defines the TX PRBS generator ports.

Table 6-14: **TX PRBS Generator Ports**

Port	Direction	Clock Domain	Description
TXENPRBSTST0[1:0] TXENPRBSTST1[1:0]	In	TXUSRCLK2	Transmitter test pattern generation control. A pseudo-random bit sequence (PRBS) is generated by enabling the test pattern generation circuit. `00`: Test pattern generation off (standard operation mode) `01`: Enable $2^7 - 1$ PRBS generation `10`: Enable $2^{23} - 1$ PRBS generation `11`: Enable $2^{31} - 1$ PRBS generation Because PRBS patterns are deterministic, the receiver can check the received data against a sequence of its own PRBS generator.

There are no attributes in this section.

Description

Each GTX transceiver includes a built-in PRBS generator. This feature can be used in conjunction with other test features, such as loopback and the built-in PRBS checker, to run tests on a given channel.

To use the PRBS generator, the PRBS test mode is selected using the TXENPRBSTST port. Table 6-14 lists the available settings.

XC2V250-5FF896C	2001+	BGA	2315
XC2V250-5FF1517I	2001+	BGA	2315
XC2V250-5FF1517C	2001+	BGA	2315
XC2V250-5FF1152I	2001+	BGA	2315
XC2V250-5FF1152C	2001+	BGA	2315
XC2V250-5CSG144I	2001+	BGA	2315
XC2V250-5CSG144C	2001+	BGA	2315
XC2V250-5CS144I	2001+	QFP	2315
XC2V250-5CS144C	2001+	BGA	2315
XC2V250-5CS144	2001+	BGA	2315
XC2V250-5BG728I	2001+	BGA	2315
XC2V250-5BG728C	2001+	BGA	2315
XC2V250-5BG575I	2001+	BGA	2315
XC2V250-5BG575C	2001+	BGA	2315
XC2V250-5BF957I	2001+	BGA	2315
XC2V250-5BF957C	2001+	BGA	2315
XC2V250-4FGG456I	2001+	BGA	2315
XC2V250-4FGG456C	2001+	BGA	2315
XC2V250-4FGG256I	2001+	BGA256	2315
XC2V250-4FGG256C	2001+	BGA144	2315
XC2V250-4FGG256	2001+	BGA	2315
XC2V250-4FG456I	2001+	BGA456	2315
XC2V250-4FG456C	2001+	BGA	2315
XC2V2504FG456C	2001+	BGA	2315
XC2V250-4FG456AFT	2001+	BGA	2315
XC2V250-4FG456	2001+	原厂原封	2315
XC2V250-4FG456	2001+	BGA	2315
XC2V250-4FG256I	2001+	QFP256	2315
XC2V250-4FG256C	2001+	BGA256	2315
XC2V250-4FG256	2001+	原厂原封	2315
XC2V250-4FG256	2001+	BGA	2315
XC2V250-4FF896I	2001+	BGA	2315
XC2V250-4FF896C	2001+	BGA	2315
XC2V250-4FF1517I	2001+	BGA	2315
XC2V250-4FF1517C	2001+	BGA	2315
XC2V250-4FF1152I	2001+	BGA	2315
XC2V250-4FF1152C	2001+	BGA	2315
XC2V250-4CSG144I	2001+	BGA144	2315
XC2V250-4CSG144C	2001+	BGA	2315
XC2V250-4CS144I	2001+	BGA144	2315
XC2V250-4CS144C	2001+	BGA	2315

XC2V250-3FG456I	2001+	原厂原封	2315
XC2V250-3FG456C	2001+	BGA	2315
XC2V250-3FG256I	2001+	BGA	2315
XC2V250-3FG256C	2001+	BGA	2315
XC2V250-2FG456C	2001+	BGA	2315
XC2V250-2FG256C	2001+	原厂原封	2315
XC2V250-	2001+	BGA	2315
XC2V250	2001+	BGA	2315
XC2V20-5FGG676I	2001+	BGA	2315
XC2V200FG676	2001+	BGA	2315
XC2V200E-7PQ240C	2001+	QFP	2315
XC2V200-6FG456C	2001+	BGA	2315
XC2V200-6FG256C	2001+	BGA	2315
XC2V200-5BG575I	2001+	BGA	2315
XC2V200-4PQ240C	2001+	44-PLCC	2315
XC2V200-4FG676I	2001+	BGA	2315
XC2V2000FGG676	2001+	BGA	2315
XC2V2000FG676AGT-5C	2001+	BGA	2315
XC2V2000-FG676AGT	2001+	BGA	2315
XC2V2000FG676AGT	2001+	BGA	2315
XC2V2000FG676-4C	2001+	BGA	2315
XC2V2000FG676 4C	2001+	BGA	2315
XC2V2000-FG676	2001+	BGA	2315
XC2V2000FG676	2001+	BGA	2315
XC2V2000-FF896AGT	2001+	BGA	2315
XC2V2000FF896	2001+	BGA	2315
XC2V2000BG676	2001+	BGA	2315
XC2V2000-BG576C	2001+	BGA	2315
XC2V2000-BG575C	2001+	BGA	2315
XC2V2000BG575	2001+	BGA	2315
XC2V2000BF957AMT	2001+	BGA	2315
XC2V2000BF957AGT	2001+	BGA	2315
XC2V2000BF957-5C	2001+	BGA	2315
XC2V2000BF957-4I	2001+	BGA	2315
XC2V2000-BF957	2001+	PBGA	2315
XC2V2000BF957	2001+	BGA	2315
XC2V2000-7FG676I	2001+	BGA	2315
XC2V2000-7FG676C	2001+	BGA	2315
XC2V2000-6FGG676I	2001+	BGA	2315
XC2V2000-6FGG676C	2001+	BGA	2315
XC2V2000-6FG676I	2001+	BGA	2315