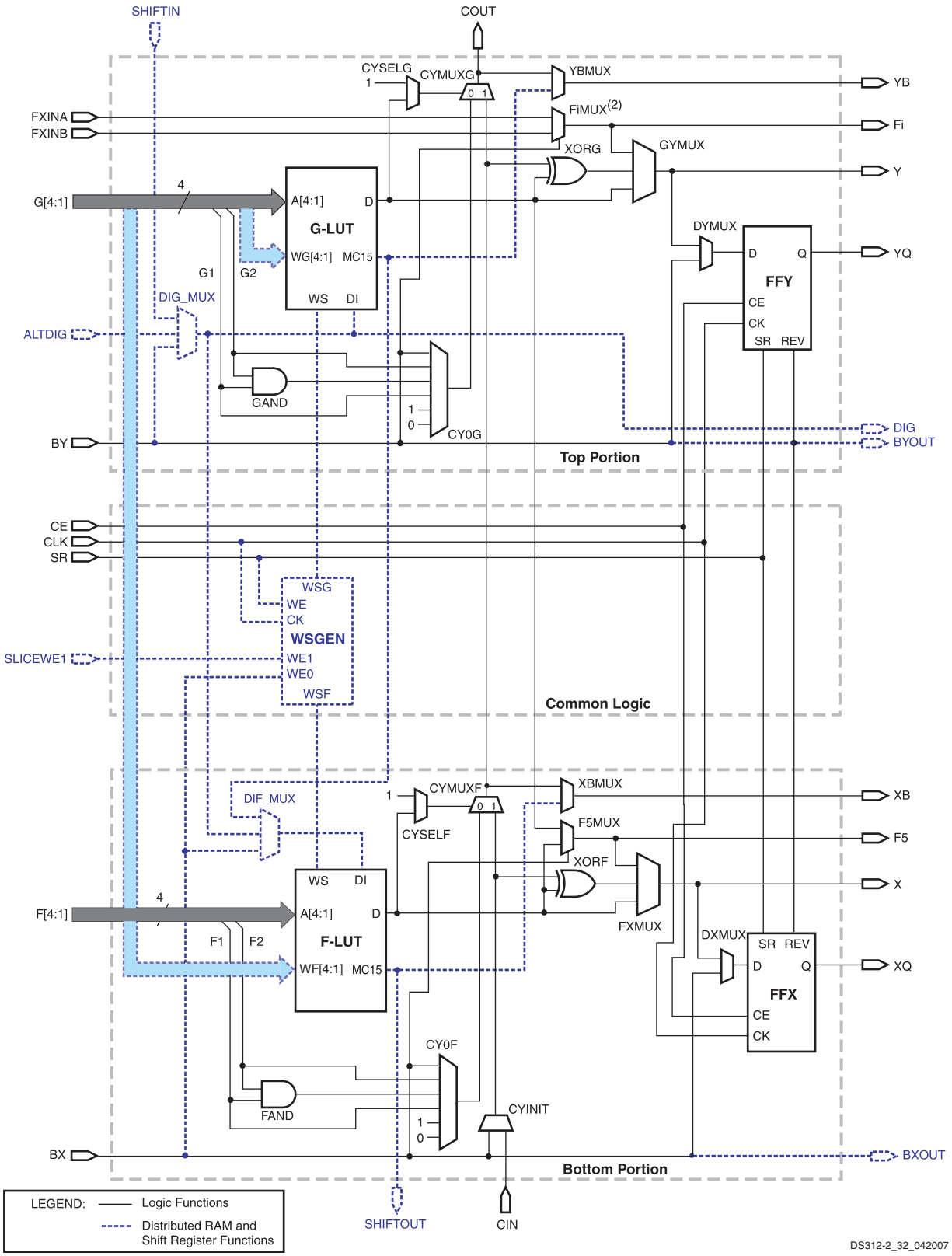
Spartan-3 FPGA Design Documentation

The functionality of the Spartan®-3 FPGA family is described in the following documents. The topics covered in each guide are listed.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

For specific hardware examples, see the Spartan-3 FPGA Starter Kit board web page, which has links to various design examples and the user guide.



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 12: **Simplified Diagram of the Left-Hand SLICEM**

XC2V2000-5F676C	2001+	BGA	2315
XC2V2000-5CS144I	2001+	BGA	2315
XC2V2000-5CS144C	2001+	BGA	2315
XC2V2000-5C/FF896	2001+	BGA	2315
XC2V2000-5C/BG576	2001+	BGA	2315
XC2V2000-5BGG728I	2001+	BGA	2315
XC2V2000-5BGG728C	2001+	原厂原封	2315
XC2V2000-5BGG575I	2001+	BGA	2315
XC2V2000-5BGG575C	2001+	BGA	2315
XC2V2000-5BG728I	2001+	BGA	2315
XC2V2000-5BG728C	2001+	NA	2315
XC2V2000-5BG575I	2001+	BGA	2315
XC2V2000-5BG575C	2001+	BGA	2315
XC2V2000-5BG575	2001+	原厂原封	2315
XC2V2000-5BG575	2001+	BGA	2315
XC2V2000-5BFG957I	2001+	BGA957	2315
XC2V2000-5BFG957C	2001+	BGA957	2315
XC2V2000-5BF957I	2001+	BGA	2315
XC2V2000-5BF957C	2001+	BGA	2315
XC2V2000-4IFF676	2001+	BGA	2315
XC2V2000-4FGG676I	2001+	BGA	2315
XC2V2000-4FGG676C	2001+	BGA	2315
XC2V2000-4FG957C	2001+	BGA	2315
XC2V2000-4FG67C	2001+	BGA-676	2315
XC2V2000-4FG676I0939	2001+	aa	2315
XC2V2000-4FG676I	2001+	BGA	2315
XC2V20004FG676I	2001+	NA	2315
XC2V2000-4FG676C	2001+	BGA	2315
XC2V20004FG676A	2001+	BGA	2315
XC2V2000-4FG676	2001+	BGA	2315
XC2V2000-4FG456I	2001+	BGA	2315
XC2V2000-4FG456C	2001+	BGA	2315
XC2V2000-4FG256I	2001+	BGA	2315
XC2V2000-4FG256C	2001+	BGA	2315
XC2V2000-4FFG896I	2001+	BGA896	2315
XC2V2000-4FFG896C	2001+	BGA	2315
XC2V2000-4FFG676I	2001+	BGA	2315
XC2V2000-4FFG676C	2001+	BGA	2315
XC2V2000-4FFF896C	2001+	BGA	2315
XC2V2000-4FF896I	2001+	BGA	2315
XC2V2000-4FF896C	2001+	BGA	2315

XC2V2000-4BGG728C	2001+	BGA	2315
XC2V2000-4BGG575I	2001+	BGA	2315
XC2V2000-4BGG575C	2001+	BGA	2315
XC2V2000-4BG957C	2001+	BGA	2315
XC2V2000-4BG728I	2001+	BGA	2315
XC2V2000-4BG728C	2001+	BGA	2315
XC2V2000-4BG728	2001+	NA	2315
XC2V2000-4BG575I	2001+	BGA	2315
XC2V2000-4BG575C	2001+	BGA	2315
XC2V2000-4BG575	2001+	BGA	2315
XC2V2000-4BFG957I	2001+	BGA	2315
XC2V2000-4BFG957C	2001+	BGA	2315
XC2V2000-4BF957I	2001+	BGA	2315
XC2V2000-4BF957C-ES	2001+	BGA	2315
XC2V2000-4BF957C0790	2001+	BGA	2315
XC2V2000-4BF957C	2001+	BGA	2315
XC2V2000-4BF957C	2001+	BGA	2315
XC2V20004BF957C	2001+	bga	2315
XC2V2000-4BF957AGT	2001+	BGA	2315
XC2V2000-4BF957	2001+	BGA957	2315
XC2V2000-4BF957	2001+	BGA	2315
XC2V2000 FG676 4C	2001+	BGA-676D	2315
XC2V2000 4FG676C	2001+	BGA	2315
XC2V2000	2001+	BGA	2315
XC2V150-6FG456C	2001+	BGA	2315
XC2V150-6FG456C	2001+	BGA	2315
XC2V1500TM-5CFG676	2001+	BGA	2315
XC2V1500FGG676	2001+	BGA	2315
XC2V1500FG676AGT-6C	2001+	BGA	2315
XC2V1500-FG676AGT	2001+	BGA	2315
XC2V1500FG676AGT	2001+	BGA	2315
XC2V1500-FG676-4C	2001+	BGA	2315
XC2V1500FG676-4C	2001+	BGA	2315
XC2V1500-FG676	2001+	BGA	2315
XC2V1500FG676	2001+	BGA	2315
XC2V1500FG575	2001+	BGA	2315
XC2V1500FFG896	2001+	BGA	2315
XC2V1500-FF896AGT	2001+	BGA	2315
XC2V1500FF896AGT	2001+	BGA	2315
XC2V1500FF896-4C	2001+	BGA	2315
XC2V1500FF896	2001+	BGA	2315

Table 45: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[3]	Max[3]	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.