require several CCLK pulses after DONE goes High. See "Startup (Step 8)" in Chapter 1 for details).

After configuration, the CS_B and RDWR_B signals can be deasserted, or they can remain asserted. Because the SelectMAP port is inactive, toggling RDWR_B at this time does not cause an abort. Figure 2-14 summarizes the timing of SelectMAP configuration with continuous data loading.
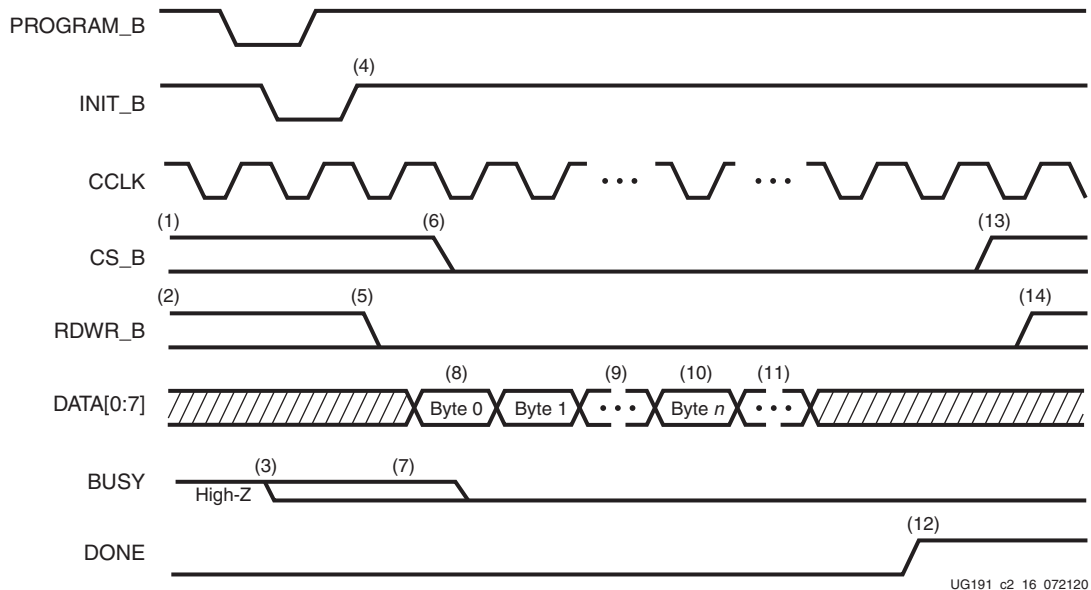

Figure 2-14: **Continuous x8 SelectMAP Data Loading**

Notes relevant to Figure 2-14:

1. CS_B signal can be tied Low if there is only one device on the SelectMAP bus. If CS_B is not tied Low, it can be asserted at any time.
2. RDWR_B can be tied Low if readback is not needed. RDWR_B should not be toggled after CS_B has been asserted because this triggers an ABORT. (See "SelectMAP ABORT").
3. If CS_B is tied Low, BUSY is driven Low before INIT_B toggles High.
4. The Mode pins are sampled when INIT_B goes High.
5. RDWR_B should be asserted before CS_B to avoid causing an abort.
6. CS_B is asserted, enabling the SelectMAP interface.
7. BUSY remains in High-Z state until CS_B is asserted.
8. The first byte is loaded on the first rising CCLK edge after CS_B is asserted.
9. The configuration bitstream is loaded one byte per rising CCLK edge.
10. After the last byte is loaded, the device enters the startup sequence.
11. The startup sequence lasts a minimum of eight CCLK cycles. (See "Startup (Step 8)" in Chapter 1.)
12. The DONE pin goes High during the startup sequence. Additional CCLKs can be required to complete the startup sequence. (See "Startup (Step 8)" in Chapter 1.)
13. After configuration has finished, the CS_B signal can be deasserted.
14. After the CS_B signal is deasserted, RDWR_B can be deasserted.
15. The data bus can be x8, x16, or x32.

Table 2-9: **Virtex-5 Device BPI Configuration Interface Pins** *(Continued)*

Pin Name	Type	Dedicated or Dual-Purpose	Description
INIT_B	Input or Output, Open-Drain	Dedicated	Before the Mode pins are sampled, INIT_B is an input that can be held Low to delay configuration. After the Mode pins are sampled, INIT_B is an open-drain, active-Low output indicating whether a CRC error occurred during configuration: 0 = CRC error 1 = No CRC error When the SEU detection function is enabled, INIT_B is optionally driven Low when a read back CRC error is detected.
PROGRAM_B	Input	Dedicated	Active-Low asynchronous full-chip reset
CCLK	Output	Dedicated	Configuration clock output. CCLK does not directly connect to BPI Flash but is used internally to generate the address and sample read data.
FCS_B	Output	Dual	Active-Low Flash chip select output. This output is actively driven Low during configuration and 3-stated after configuration. It has a weak pull-up resistor during configuration. By default, this signal has a weak pull-down resistor after configuration.
FOE_B	Output	Dual	Active-Low Flash output enable. This output is actively driven Low during configuration and 3-stated after configuration. It has a weak pull-up resistor during configuration. By default, this signal has a weak pull-down resistor after configuration.
FWE_B	Output	Dual	Active-Low Flash write enable. This output is actively driven High during configuration and 3-stated after configuration. It has a weak pull-up resistor during configuration. By default, this signal has a weak pull-down resistor after configuration.
ADDR[25:0]	Output	Dual	Address output. For I/O bank locations, see Table 1-2, page 17.
D[15:0]	Input	Dual	Data input, sampled by the rising edge of the FPGA CCLK. For I/O bank location, see Table 1-2, page 17.

XC2V1500-6FF1152I	2001+	BGA	2315
XC2V1500-6FF1152C	2001+	BGA	2315
XC2V1500-6CS144I	2001+	BGA	2315
XC2V1500-6CS144C	2001+	BGA	2315
XC2V1500-6BGG575I	2001+	BGA	2315
XC2V1500-6BGG575C	2001+	BGA	2315
XC2V15006BGG575C	2001+	NA	2315
XC2V1500-6BG728I	2001+	BGA	2315
XC2V1500-6BG728C	2001+	BGA	2315
XC2V1500-6BG575I	2001+	BGA	2315
XC2V1500-6BG575C	2001+	BGA	2315
XC2V1500-6BF957I	2001+	BGA	2315
XC2V1500-6BF957C	2001+	BGA	2315
XC2V1500676	2001+	BGA	2315
XC2V1500-5FT896C	2001+	原厂原封	2315
XC2V1500-5FGG676I	2001+	BGA676	2315
XC2V1500-5FGG676C	2001+	BGA	2315
XC2V1500-5FG676I	2001+	BGA	2315
XC2V15005FG676I	2001+	NA	2315
XC2V1500-5FG676C	2001+	BGA676	2315
XC2V1500-5FG6761	2001+	BGA	2315
XC2V1500-5FG575C	2001+	BGA	2315
XC2V1500-5FG456I	2001+	BGA	2315
XC2V1500-5FG456C	2001+	BGA	2315
XC2V1500-5FG256I	2001+	BGA	2315
XC2V1500-5FG256C	2001+	BGA	2315
XC2V1500-5FFG896I	2001+	BGA	2315
XC2V1500-5FFG896C	2001+	BGA	2315
XC2V1500-5FF896I	2001+	BGA	2315
XC2V1500-5FF896C	2001+	BGA	2315
XC2V1500-5FF1517I	2001+	BGA	2315
XC2V1500-5FF1517C	2001+	BGA	2315
XC2V1500-5FF1152I	2001+	BGA	2315
XC2V1500-5FF1152C	2001+	BGA	2315
XC2V1500-5CS144I	2001+	BGA	2315
XC2V1500-5CS144C	2001+	BGA	2315
XC2V1500-5BGG575I	2001+	BGA	2315
XC2V1500-5BGG575C	2001+	BGA	2315
XC2V1500-5BG728I	2001+	BGA	2315
XC2V1500-5BG728C	2001+	BGA	2315
XC2V1500-5BG575I	2001+	BGA	2315

XC2V15004FG676C	2001+	BGA	2315
XC2V1500-4FG676	2001+	BGA	2315
XC2V1500-4FG456I	2001+	BGA	2315
XC2V1500-4FG456C	2001+	BGA	2315
XC2V1500-4FG256I	2001+	BGA	2315
XC2V1500-4FG256C	2001+	BGA	2315
XC2V1500-4FFG896I	2001+	BGA	2315
XC2V1500-4FFG896C	2001+	BGA896	2315
XC2V1500-4FFG676	2001+	BGA	2315
XC2V1500-4FF896I	2001+	BGA896	2315
XC2V1500-4FF896C	2001+	BGA896	2315
XC2V15004FF896C	2001+	BGA	2315
XC2V1500-4FF896	2001+	BGA	2315
XC2V1500-4FF1517I	2001+	BGA	2315
XC2V1500-4FF1517C	2001+	BGA	2315
XC2V1500-4FF1152I	2001+	BGA	2315
XC2V1500-4FF1152C	2001+	BGA	2315
XC2V1500-4CS144I	2001+	BGA	2315
XC2V1500-4CS144C	2001+	BGA	2315
XC2V1500-4BGG575I	2001+	BGA	2315
XC2V1500-4BGG575C	2001+	BGA	2315
XC2V1500-4BG728I	2001+	BGA	2315
XC2V1500-4BG728C	2001+	BGA	2315
XC2V1500-4BG575I	2001+	BGA	2315
XC2V1500-4BG575C	2001+	BGA	2315
XC2V1500-4BG575AGT	2001+	BGA	2315
XC2V15004BG575	2001+	BGA	2315
XC2V1500-4BF957I	2001+	BGA	2315
XC2V1500-4BF957C	2001+	BGA	2315
XC2V1500 FF896 4C	2001+	BGA-896	2315
XC2V1500	2001+	BGA	2315
XC2V100FG456BGT	2001+	BGA	2315
XC2V100E-5PQG208I	2001+	原厂原封	2315
XC2V100E-5PQ208I	2001+	QFP	2315
XC2V100E-4PQG208I	2001+	QFP	2315
XC2V100-CFG456C	2001+	BGA	2315
XC2V1000TM-FGG456AGT	2001+	BGA	2315
XC2V1000TMFF896	2001+	BGA	2315
XC2V1000TM4FG256AGTC	2001+	BGA	2315
XC2V1000TM4BG575AFTC	2001+	BGA	2315
XC2V1000TM	2001+	N/A	2315

TAP Controller

Figure 3-2 diagrams a 16-state finite state machine. The four TAP pins control how data is scanned into the various registers. The state of the TMS pin at the rising edge of TCK determines the sequence of state transitions. There are two main sequences, one for shifting data into the data register and the other for shifting an instruction into the instruction register.

A transition between the states only occurs on the rising edge of TCK, and each state has a different name. The two vertical columns with seven states each represent the Instruction Path and the Datapath. The data registers operate in the states whose names end with "DR," and the instruction register operates in the states whose names end in "IR." The states are otherwise identical.

The operation of each state is described below.

Test-Logic-Reset:
All test logic is disabled in this controller state, enabling the normal operation of the IC. The TAP controller state machine is designed so that regardless of the initial state of the controller, the Test-Logic-Reset state can be entered by holding TMS High and pulsing TCK five times. Consequently, the Test Reset (TRST) pin is optional.

Run-Test-Idle:
In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it is executed when the controller enters this state. The test logic in the IC is idle otherwise.

Select-DR-Scan:
This controller state controls whether to enter the Datapath or the Select-IR-Scan state.

Select-IR-Scan:
This controller state controls whether or not to enter the Instruction Path. The controller can return to the Test-Logic-Reset state otherwise.

Capture-IR:
In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits must always be 01.

Shift-IR:
In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

Exit1-IR:
This controller state controls whether to enter the Pause-IR state or Update-IR state.

Pause-IR:
This state allows the shifting of the instruction register to be temporarily halted.

Exit2-DR:
This controller state controls whether to enter either the Shift-IR state or Update-IR state.

Update-IR:
In this controller state, the instruction in the instruction register is latched to the latch bank of the Instruction Register on every falling edge of TCK. This instruction becomes the current instruction after it is latched.