- Spartan-6 FPGA Clocking Resources User Guide

  This guide describes the clocking resources available in all Spartan-6 devices, including the DCMs and the PLLs.

- Spartan-6 FPGA Block RAM Resources User Guide

  This guide describes the Spartan-6 device block RAM capabilities.

- Spartan-6 FPGA Configurable Logic Blocks User Guide

  This guide describes the capabilities of the configurable logic blocks (CLBs) available in all Spartan-6 devices.

- Spartan-6 FPGA Memory Controller User Guide

  This guide describes the Spartan-6 FPGA memory controller block, a dedicated, embedded multi-port memory controller that greatly simplifies interfacing Spartan-6 FPGAs to the most popular memory standards.

- Spartan-6 FPGA GTP Transceivers User Guide

  This guide describes the GTP transceivers available in Spartan-6 LXT FPGAs.

- Spartan-6 FPGA DSP48A1 Slice User Guide

  This guide describes the architecture of the DSP48A1 slice in Spartan-6 FPGAs and provides configuration examples.

- Spartan-6 FPGA PCB and Pin Planning Design Guide

  This guide provides information on PCB design for Spartan-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

- Spartan-6 FPGA Power Management User Guide

  This guide provides information on the various hardware methods of power management in Spartan-6 devices, primarily focusing on the suspend mode.

Additional Resources

Chapter 1

Configuration Overview

Overview

Spartan®-6 FPGAs are configured by loading application-specific configuration data—a bitstream—into internal memory. Spartan-6 FPGAs can load themselves from an external nonvolatile memory device or they can be configured by an external smart source, such as a microprocessor, DSP processor, microcontroller, PC, or board tester. In any case, there are two general configuration datapaths. The first is the serial datapath that is used to minimize the device pin requirements. The second datapath is the 8- or 16-bit datapath used for higher performance or access (or link) to industry-standard interfaces, ideal for external data sources like processors, or x8- or x16-parallel flash memory.

Like processors and processor peripherals, Xilinx® FPGAs can be reprogrammed, in system, on demand, an unlimited number of times.

Because Xilinx FPGA configuration data is stored in CMOS configuration latches (CCLs), it must be reconfigured after it is powered down. The bitstream is loaded each time into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes:

- JTAG configuration mode
- Master Serial/SPI configuration mode (x1, x2, and x4)
- Slave Serial configuration mode
- Master SelectMAP/BPI configuration mode (x8 and x16)
- Slave SelectMAP configuration mode (x8 and x16)

The configuration modes are explained in detail in Chapter 2, Configuration Interface Basics.

The specific configuration mode is selected by setting the appropriate level on the mode input pins M[1:0]. The M1 and M0 mode pins should be set at a constant DC voltage level and tied directly to ground or VCCO_2. The mode pins should not be toggled during or before configuration but can be toggled after. See Chapter 2, Configuration Interface Basics, for the mode pin setting options.

The terms Master and Slave refer to the direction of the configuration clock (CCLK):

- In Master configuration modes, the Spartan-6 device drives CCLK from an internal oscillator by default or optional external master clock source GCLK0/USERCCLK. To select the desired frequency, the BitGen **`-g ConfigRate`** option is used for the internal oscillator. The default is 2 MHz. The CCLK output frequency varies with process, voltage, and temperature. The data sheet $F_{MCCKTOL}$ specification defines the frequency tolerance. A frequency tolerance of ±50% means that a ConfigRate setting of 10 could generate a CCLK rate of between 5 MHz and 15 MHz.The BitGen section

XC2V1000-5FG256I	2001+	BGA	2315
XC2V1000-5FG256C	2001+	BGA	2315
XC2V1000-5FG256	2001+	原厂原封	2315
XC2V1000-5FFG896I	2001+	BGA	2315
XC2V1000-5FFG896C	2001+	BGA	2315
XC2V1000-5FFG456I	2001+	BGA	2315
XC2V1000-5FF896I	2001+	BGA	2315
XC2V10005FF896C0765	2001+	BGA	2315
XC2V1000-5FF896C ES	2001+	BGA	2315
XC2V1000-5FF896C	2001+	BGA	2315
XC2V1000-5FF896C	2001+	BGA	2315
XC2V1000-5FF896C	2001+	BGA	2315
XC2V1000-5FF896	2001+	原厂原封	2315
XC2V1000-5FF896	2001+	BGA	2315
XC2V1000-5FF1704C	2001+	BGAQFP	2315
XC2V1000-5FF1517I	2001+	BGA	2315
XC2V1000-5FF1517C	2001+	BGA	2315
XC2V1000-5FF1152I	2001+	BGA	2315
XC2V1000-5FF1152C	2001+	BGA	2315
XC2V1000-5CS144I	2001+	BGA	2315
XC2V1000-5CS144C	2001+	BGA	2315
XC2V1000-5C/FG456	2001+	BGA	2315
XC2V1000-5BGG575I	2001+	BGA	2315
XC2V1000-5BGG575C	2001+	BGA	2315
XC2V10005BGG575C	2001+	BGA	2315
XC2V1000-5BG728I	2001+	BGA	2315
XC2V1000-5BG728C	2001+	BGA	2315
XC2V1000-5BG575I	2001+	BGA	2315
XC2V1000-5BG575C	2001+	BGA	2315
XC2V10005BG575C	2001+	BGA	2315
XC2V1000-5BG575	2001+	BGA	2315
XC2V1000-5BG57	2001+	BGA	2315
XC2V1000-5BF957I	2001+	BGA	2315
XC2V1000-5BF957C	2001+	BGA	2315
XC2V1000-4IFG256	2001+	BGA	2315
XC2V1000-4FGG456I	2001+	BGA	2315
XC2V1000-4FGG456I	2001+	BGA	2315
XC2V1000-4FGG456C	2001+	BGA	2315
XC2V1000-4FGG256I	2001+	BGA256	2315
XC2V1000-4FGG256C	2001+	BGA	2315
XC2V1000-4FG676I	2001+	BGA	2315

XC2V1000-4FG456C	2001+	BGA	2315
XC2V10004FG456C	2001+	BGA	2315
XC2V1000-4FG456AGT	2001+	FBGA-456	2315
XC2V1000-4FG456AFT	2001+	BGA	2315
XC2V1000-4FG456	2001+	BGA	2315
XC2V10004FG456	2001+	BGA	2315
XC2V1000-4FG456	2001+	BGA	2315
XC2V1000-4FG256I	2001+	BGA	2315
XC2V1000-4FG256I	2001+	BGA	2315
XC2V1000-4FG256CR02	2001+	BGA256	2315
XC2V1000-4FG256C-ES	2001+	BGA	2315
XC2V1000-4FG256C0921	2001+	BGA	2315
XC2V1000-4FG256C	2001+	BGA	2315
XC2V1000-4FG256	2001+	BGA	2315
XC2V1000-4FG256	2001+	BGA	2315
XC2V1000-4FFG896I	2001+	BGA	2315
XC2V1000-4FFG896C	2001+	BGA	2315
XC2V1000-4FF896I	2001+	BGA	2315
XC2V1000-4FF896C-ES	2001+	BGA-896	2315
XC2V1000-4FF896C	2001+	BGA896	2315
XC2V1000-4FF896C	2001+	BGA	2315
XC2V10004FF896C	2001+	BGA	2315
XC2V1000-4FF896	2001+	BGA	2315
XC2V1000-4FF256C	2001+	BGA	2315
XC2V1000-4FF1517I	2001+	BGA	2315
XC2V1000-4FF1517C	2001+	BGA	2315
XC2V1000-4FF1152I	2001+	BGA	2315
XC2V1000-4FF1152C	2001+	BGA	2315
XC2V1000-4CS144I	2001+	BGA	2315
XC2V1000-4CS144C	2001+	BGA	2315
XC2V1000-4CFGG456	2001+	BGA	2315
XC2V1000-4CFGG256	2001+	BGA	2315
XC2V1000-4C/FF896	2001+	BGA	2315
XC2V1000-4BGG575I	2001+	BGA	2315
XC2V10004BGG575I	2001+	BGA	2315
XC2V1000-4BGG575C	2001+	BGA	2315
XC2V1000-4BG728I	2001+	BGA	2315
XC2V1000-4BG728C	2001+	BGA	2315
XC2V1000-4BG575I	2001+	BGA	2315
XC2V1000-4BG575I	2001+	BGA	2315
XC2V1000-4BG575C-ES	2001+	BGA	2315

supply sequencing requirements. Power V_{CCO} last after V_{CCINT} and V_{CCAUX} to ensure that the outputs stay disabled until configuration begins.

All JTAG and serial configuration pins are located in V_{CCAUX} and VCCO_2 supply banks. The dual-purpose pins are located in Banks 0, 1, and 2 (one exception is A24 and A25 are in bank 5 for larger devices with 6 I/O banks). The DONE and PROGRAM_B dedicated inputs operate at the VCCO_2 LVCMOS level, and the JTAG input pins (TCK, TMS, and TDI) and the SUSPEND pin operate at the V_{CCAUX} LVCMOS level. The DONE pin operates at the VCCO_2 voltage level with the output standard set to LVCMOS 8 mA SLOW. TDO drives at the voltage level provided on V_{CCAUX} at 8 mA SLOW.

For all modes that use dual-purpose I/O, the associated VCCO_X must be connected to the appropriate voltage to match the I/O standard of the configuration device. HSWAPEN requires that VCCO_0 be supplied, and DOUT requires that VCCO_1 be supplied. The pins are also LVCMOS18, LVCMOS25, or LVCMOS33 8 mA SLOW during configuration, depending on the VCCO_X level.

For power-up, the V_{CCINT} power pins must be supplied with 1.2V for -2/-3 speed grades and 1.0V for -1L sources. VCCO_2 must be supplied. Table 5-11 shows the power supplies required for configuration. Table 5-12 shows the timing for power-up.

Table 5-11: **Power Supplies Required for Configuration**

Pin Name[1]	Description
V_{CCINT}	Internal core voltage.
V_{BATT}[2]	Encryption Key battery supply. If there is no encryption key being stored in the volatile memory, V_{BATT} should be connected to V_{CCAUX} or GND, or left unconnected.
V_{FS}	Encryption Key eFUSE programming voltage. If eFUSE programming is not needed, connect V_{FS} to V_{CC} or GND (recommended).
V_{CCAUX}[3]	Auxiliary power input for configuration logic and other FPGA functions.
VCCO_0 VCCO_1 VCCO_2[4] VCCO_5[5]	Dual-purpose configuration pin output supply voltage. VCCO_2 cannot be 1.2V or 1.5V during configuration.

Notes:

1. For recommended operating values, refer to DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*.
2. V_{BATT} or V_{FS} are required only when using bitstream encryption and are only supported in Spartan-6 LX75, LX75T, LX100, LX100T, LX150, and LX150T devices.
3. V_{CCAUX} must be greater than or equal to V_{FS} during eFUSE programming. This requirement is not necessary for configuration.
4. If VCCO_2 is 1.8V, V_{CCAUX} must be 2.5V. If VCCO_2 is 2.5V or 3.3V, V_{CCAUX} can be either 2.5V or 3.3V.
5. VCCO_5 might be needed if BPI configuration mode is used and A24 and A25 are in I/O Bank 5.