Non-Continuous SelectMAP Data Loading

Non-continuous data loading is used in applications where the configuration controller cannot provide an uninterrupted stream of configuration data—for example, if the controller pauses configuration while it fetches additional data.

Configuration can be paused in two ways: by deasserting the CS_B signal (Free-Running CCLK method, Figure 2-15) or by halting CCLK (Controlled CCLK method, Figure 2-16).
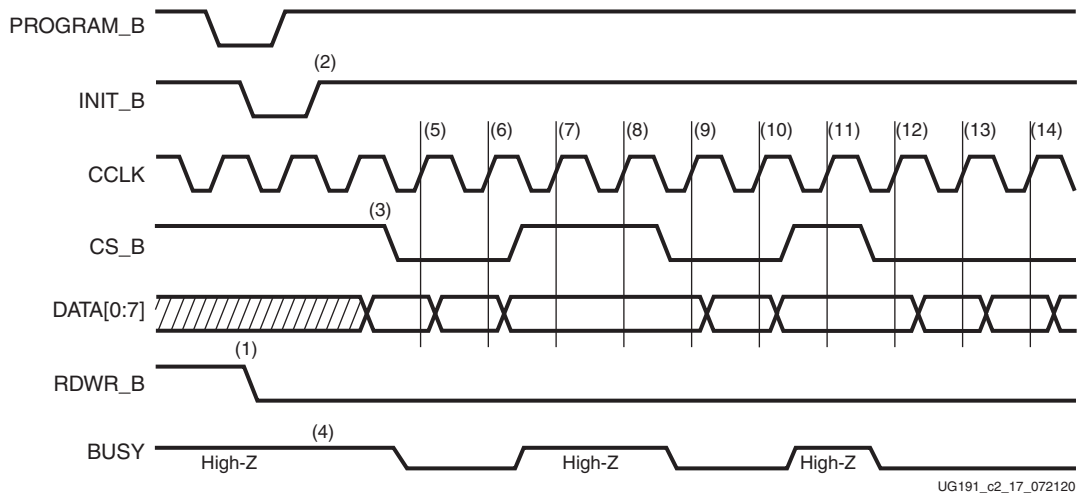

Figure 2-15:   **Non-Continuous SelectMAP Data Loading with Free-Running CCLK**

Notes relevant to Figure 2-15:

1. RDWR_B is driven Low by the user, setting the D[0:7] pins as inputs for configuration. RDWR_B can be tied Low if readback is not needed. RDWR_B should not be toggled after CS_B has been asserted because this triggers an ABORT. (See "SelectMAP ABORT").

2. The device is ready for configuration after INIT_B toggles High.

3. The user asserts CS_B Low, enabling the SelectMAP data bus. CS_B signal can be tied Low if there is only one device on the SelectMAP bus. If CS_B is not tied Low, it can be asserted at any time.

4. BUSY goes Low shortly after CS_B is asserted. If CS_B is tied Low, BUSY is driven Low before INIT_B toggles High.

5. A byte is loaded on the rising CCLK edge. The data bus can be x8, x16, or x32 wide.

6. A byte is loaded on the rising CCLK edge.

7. The user deasserts CS_B, and the byte is ignored.

8. The user deasserts CS_B, and the byte is ignored.

9. A byte is loaded on the rising CCLK edge.

10. A byte is loaded on the rising CCLK edge.

11. The user deasserts CS_B, and the byte is ignored.

12. A byte is loaded on the rising CCLK edge.

13. A byte is loaded on the rising CCLK edge.

14. A byte is loaded on the rising CCLK edge.

XC2V1000-3FG456C	2001+	BGA	2315
XC2V1000-3FG256I	2001+	BGA	2315
XC2V1000-3FG256C	2001+	BGA	2315
XC2V1000-3BG575C	2001+	BGA	2315
XC2V1000-2FG456	2001+	BGA	2315
XC2V1000-1FG456C	2001+	BGA	2315
XC2V1000/FF896	2001+	BGA-896D	2315
XC2V1000 FG456 4I	2001+	BGA-456D	2315
XC2V1000　5FG456C	2001+	BGA	2315
XC2V1000　FG456	2001+	BGA	2315
XC2V1000	2001+	BGA	2315
XC2S64VQ100	2001+	QFP	2315
XC2S64AVQ44	2001+	QFP	2315
XC2S64-7VQ100	2001+	QFP	2315
XC2S64-6VQ100	2001+	QFP	2315
XC2S600F-FG676AGT	2001+	PGA	2315
XC2S600ETM	2001+	N A	2315
XC2S600E-FGG676C	2001+	BGA	2315
XC2S600EFGG676	2001+	BGA	2315
XC2S600EFGF676	2001+	BGA	2315
XC2S600E-FG676C	2001+	BGA	2315
XC2S600EFG676AGT	2001+	BGA	2315
XC2S600E-FG676-6C	2001+	BGA	2315
XC2S600EFG676-6C	2001+	BGA	2315
XC2S600E-FG676	2001+	BGA	2315
XC2S600EFG676	2001+	BGA	2315
XC2S600EFG456GAT	2001+	BGA	2315
XC2S600E-FG456AGT	2001+	BGA	2315
XC2S600EFG456AGT	2001+	BGA	2315
XC2S600E-FG456AG	2001+	BGA	2315
XC2S600EFG456-7Q/7C	2001+	BGA	2315
XC2S600EFG456-6I	2001+	BGA	2315
XC2S600E-FG456	2001+	BGA	2315
XC2S600EFG456	2001+	BGA	2315
XC2S600E-7TQG144I	2001+	BGA	2315
XC2S600E-7TQG144C	2001+	BGA	2315
XC2S600E-7TQ144I	2001+	BGA	2315
XC2S600E-7TQ144C	2001+	BGA	2315
XC2S600E-7PQG208I	2001+	BGA	2315
XC2S600E-7PQG208C	2001+	BGA	2315
XC2S600E-7PQ208I	2001+	BGA	2315

|			
XC2S600E-7FT256C	2001+	BGA	2315
XC2S600E-7FGG676I	2001+	BGA	2315
XC2S600E-7FGG676C	2001+	BGA	2315
XC2S600E-7FGG456I	2001+	BGA	2315
XC2S600E-7FGG456C	2001+	BGA	2315
XC2S600E-7FG676I	2001+	BGA	2315
XC2S600E-7FG676C	2001+	BGA	2315
XC2S600E-7FG676	2001+	BGA	2315
XC2S600E-7FG456I	2001+	BGA456	2315
XC2S600E-7FG456C	2001+	BGA	2315
XC2S600E-6TQG144I	2001+	BGA	2315
XC2S600E-6TQG144C	2001+	BGA	2315
XC2S600E-6TQ144I	2001+	BGA	2315
XC2S600E-6TQ144C	2001+	BGA	2315
XC2S600E-6PQG208I	2001+	BGA	2315
XC2S600E-6PQG208C	2001+	BGA	2315
XC2S600E-6PQ208I	2001+	BGA	2315
XC2S600E-6PQ208C	2001+	BGA	2315
XC2S600E-6FTG256I	2001+	BGA	2315
XC2S600E-6FTG256C	2001+	BGA	2315
XC2S600E-6FT256I	2001+	BGA	2315
XC2S600E-6FT256C	2001+	BGA	2315
XC2S600E-6FGG676I	2001+	BGA	2315
XC2S600E-6FGG676C	2001+	BGA	2315
XC2S600E-6FGG676	2001+	BGA	2315
XC2S600E-6FGG456I	2001+	BGA	2315
XC2S600E-6FGG456C	2001+	BGA	2315
XC2S600E6FGG456C	2001+	NA	2315
XC2S600E-6FGG256C	2001+	BGA	2315
XC2S600E-6FG676I	2001+	BGA	2315
XC2S600E-6FG676CN	2001+	BGA	2315
XC2S600E-6FG676C	2001+	BGA	2315
XC2S600E-6FG676	2001+	BGA	2315
XC2S600E-6FG456Q	2001+	BGA	2315
XC2S600E-6FG456I	2001+	BGA	2315
XC2S600E-6FG456G	2001+	BGA456	2315
XC2S600E-6FG456C	2001+	BGA456	2315
XC2S600E6FG456C	2001+	BGA	2315
XC2S600E-6FG456	2001+	BGA	2315
XC2S600E-6FG256I	2001+	BGA	2315
XC2S600E-6FG256C	2001+	BGA	2315

UG191_c3_03_050406
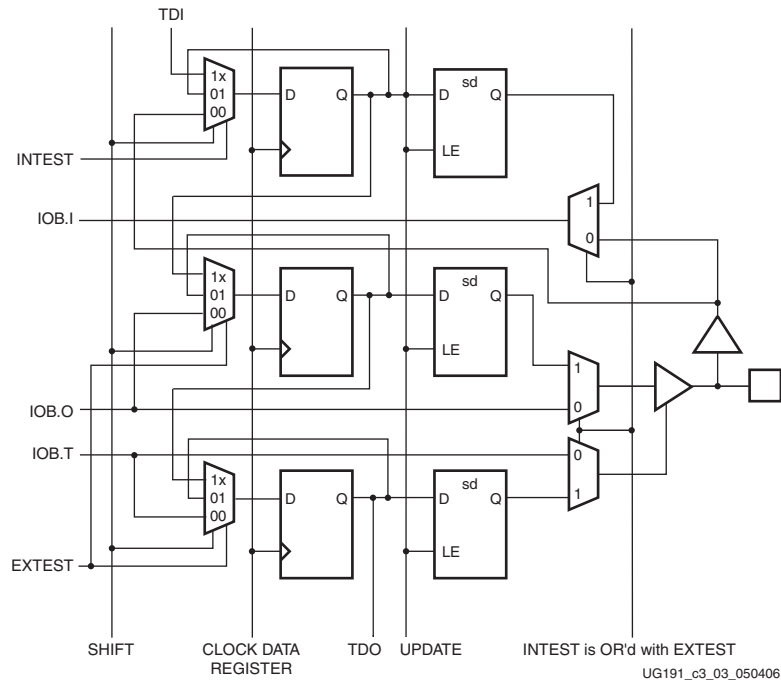
Figure 3-3: **Virtex-5 Family Boundary-Scan Logic**

Bit Sequence Boundary-Scan Register

The order of each non-TAP IOB is described in this section. The input is first, then the output, and finally the 3-state IOB control. The 3-state IOB control is closest to the TDO. The input-only pins contribute only the input bit to the Boundary-Scan I/O data register. The bit sequence of the device is obtainable from the *Boundary-Scan Description Language Files* (BSDL files) for the Virtex-5 family. (These files can be obtained from the Xilinx software download area.) The bit sequence always has the same bit order and the same number of bits and is independent of the design.

Instruction Register

The Instruction Register (IR) for the Virtex-5 device is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel-loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

To determine the operation to be invoked, an OPCODE necessary for the Virtex-5 Boundary-Scan instruction set is loaded into the Instruction Register. The length of the IR is device size-specific. The IR is 10 bits wide for the Virtex-5 LX, LXT, SXT, FXT, and TXT platform devices. The FX100T, FX130T, and FX200T have 14 bits of OPCODE because they contain 2 PowerPC processors. The 4 or 8 most significant bits support the PowerPC 440 embedded processor. The least significant 6 bits of the instruction code perform the same function for all Virtex-5 family members to support the new IEEE Standard 1532 for ISC devices. For PPC JTAG instruction, the least bits must be set to `100000` (20h). For PPC440 JTAG guidelines, refer to UG200, *Embedded Processor Block in Virtex-5 FPGAs Reference Guide*. Table 3-3 lists the available instructions for Virtex-5 devices.

TDI ∅	IR[9:6]	IR[5]	IR[4]	IR[3]	IR[2]	IR[1:0]	∅ **TDO**
	Reserved	DONE	INIT[1]	ISC_ENABLED	ISC_DONE	0 1	

Notes:

1. INIT is the status bit of the INIT_COMPLETE signal.

Figure 3-4:   **Virtex-5 Device Instruction Capture Values Loaded into IR as Part of an Instruction Scan Sequence**

BYPASS Register

The other standard data register is the single flip-flop BYPASS register. It passes data serially from the TDI pin to the TDO pin during a bypass instruction. This register is initialized to zero when the TAP controller is in the CAPTURE-DR state.

Identification (IDCODE) Register

Virtex devices have a 32-bit identification register called the IDCODE register. The IDCODE is based on the IEEE 1149.1 standard, and is a fixed, vendor-assigned value that is used to identify electrically the manufacturer and the type of device that is being addressed. This register allows easy identification of the part being tested or programmed by Boundary-Scan, and it can be shifted out for examination by using the IDCODE instruction.

The last bit of the IDCODE is always 1 (based on JTAG IEEE 1149.1). The last three hex digits appear as 0x093. IDCODEs assigned to Virtex-5 FPGAs are shown in .

JTAG Configuration Register

The JTAG Configuration register is a 32-bit register. This register allows access to the configuration bus and readback operations.

USERCODE Register

The USERCODE instruction is supported in the Virtex-5 family. This register allows a user to specify a design-specific identification code. The USERCODE can be programmed into the device and can be read back for verification later. The USERCODE is embedded into the bitstream during bitstream generation (BitGen **-g** UserID option) and is valid only after configuration. If the device is blank or the USERCODE was not programmed, the USERCODE register contains 0xFFFFFFFF.

USER1, USER2, USER3, and USER4 Registers

The USER1, USER2, USER3, and USER4 registers are only available after configuration. These four registers must be defined by the user within the design. These registers can be accessed after they are defined by the TAP pins.

The BSCAN_VIRTEX5 library macro is required when creating these registers. This symbol is only required for driving internal scan chains (USER1, USER2, USER3, and USER4).

A common input pin (TDI) and shared output pins represent the state of the TAP controller (RESET, SHIFT, and UPDATE). Virtex-5 TAP pins are dedicated and do not require the BSCAN_VIRTEX5 macro for normal Boundary-Scan instructions or operations. For HDL, the BSCAN_VIRTEX5 macro must be instantiated in the design.