PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (`CLK[15..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	`CLK` pins, PLL outputs, or internal logic	`CLK` pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between `CLKp` pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

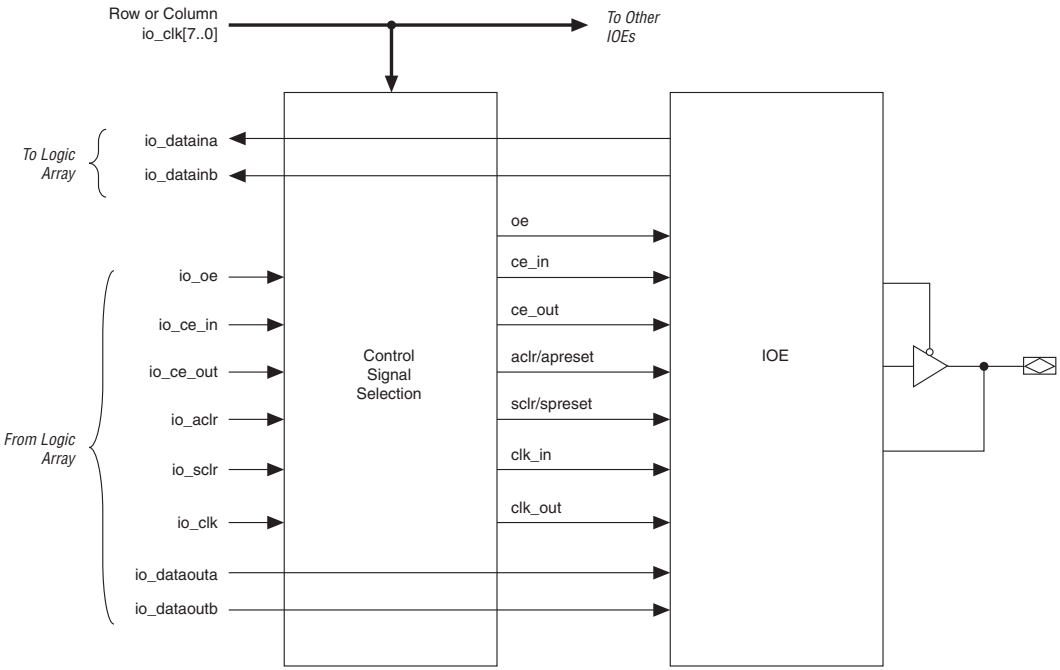
EP2AGZ300FH29I3N	4000	DIP16	20+	ALTERA
EP2AGZ300HF40I3N	1400	SOP	20+	ALTERA
EP2AGZ300HF40I4N	1500	PWRSO-10	20+	ALTERA
EP2AGZ350FF35I3N	50	BGA	20+	ALTERA
EP2AGZ350FF35I4N	14000	TSSOP20	20+	ALTERA
EP2AGZ350FH29I3N	350	SOT233	20+	ALTERA
EP2AGZ350FH29I4N	60000	DIP-8	20+	ALTERA
EP2AGZ350HF40I3N	3000	SMD	20+	ALTERA
EP2AGZ350HF40I4N	5800	SMD	20+	ALTERA
EP2S130F1020C3N	160	FCBGA	20+	ALTERA
EP2S130F1020C4N	200	BGA	20+	ALTERA
EP2S130F1020C5N	237	FCBGA1738	20+	ALTERA
EP2S130F1020I4	300	BGA	20+	ALTERA
EP2S130F1020I4N	34	BGA	20+	ALTERA/INTER
EP2S130F1020I4N	252	BGA	20+	ALTERA
EP2S15F484C4	200	FBGA	20+	ALTERA
EP2S15F484C4N	109	FBGA	20+	ALTERA
EP2S15F484C5	200	BGA	20+	ALTERA
EP2S15F484C5N	120	FCBGA	20+	ALTERA
EP2S180F1020C3	160	FCBGA	20+	ALTERA
EP2S180F1020C3N	160	FCBGA	20+	ALTERA
EP2S180F1020I4	100	BGA	20+	ALTERA
EP2S180F1020I4N	84	FBGA1517	20+	ALTERA
EP2S180F1508C3N	172	BGA	20+	ALTERA
EP2S180F1508I4	180	BGA	20+	ALTERA
EP2S180F1508I4N	280	BGA	20+	ALTERA
EP2S30F484C3N	213	FCBGA1156	20+	ALTERA
EP2S30F484C4N	56	FCBGA1157	20+	ALTERA
EP2S30F484C5N	32640	SOP	20+	ALTERA
EP2S30F484I4N	326	FCBGA1153	20+	ALTERA
EP2S30F672C5N	286	FCBGA324	20+	ALTERA
EP2S30F672I4N	105	FCBGA324	20+	ALTERA
EP2S60F1020C3N	106	FCBGA1928	20+	ALTERA
EP2S60F1020C4N	156	BGA	20+	ALTERA
EP2S60F1020C4N	40	BGA	20+	ALTERA/INTER
EP2S60F1020C5N	459	BGA	20+	ALTERA
EP2S60F1020C5N	9	BGA	20+	ALTERA/INTER

芯片详细信息

Manufacturer Part Number: EP3C80F780I8N	Pbfree Code: Yes	Rohs Code: Yes	Part Life Cycle Code: Transferred
Ihs Manufacturer: ALTERA CORP	Package Description: BGA, BGA780,28X28,40	Reach Compliance Code: compliant	Manufacturer: Altera Corporation
Risk Rank: 5.81	JESD-30 Code: S-PBGA-B780	JESD-609 Code: e1	Length: 29 mm
Number of Inputs: 429	Number of Logic Cells: 81264	Number of Outputs: 429	Number of Terminals: 780
Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA780,28X28,40	Package Shape: SQUARE
Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): NOT SPECIFIED	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2.4 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Terminal Finish: Tin/Silver/Copper (Sn/Ag/Cu)
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): NOT SPECIFIED
Width: 29 mm			

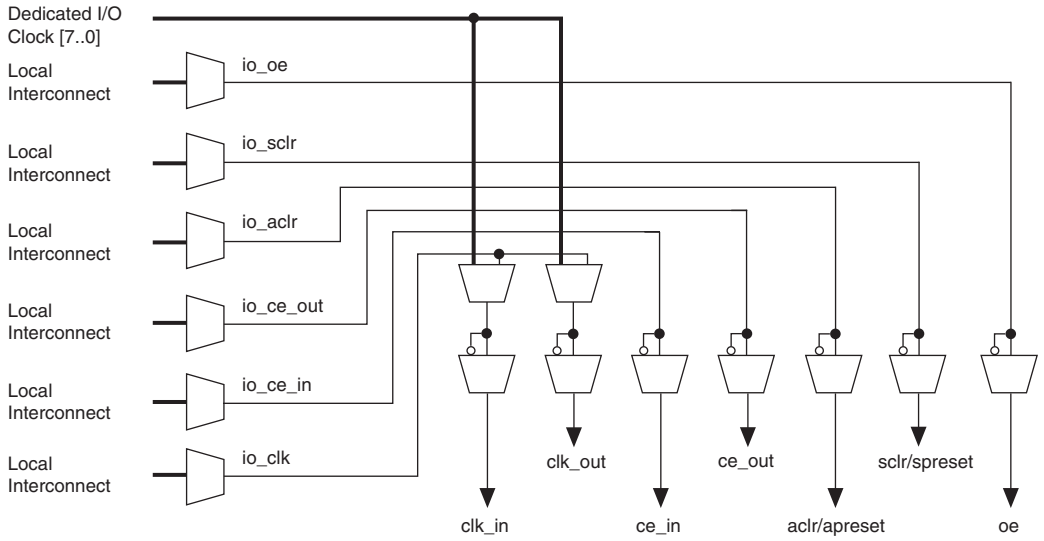
There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the "PLLs & Clock Networks" section). Figure 2–49 illustrates the signal paths through the I/O block.

Figure 2–49. Signal Path through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.

Figure 2–50. Control Signal Selection per IOE



Notes to Figure 2–50:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects.