DC Characteristics

This section lists the input pin capacitances, on-chip termination tolerance, and hot- socketing specifications.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Since these currents vary largely with the resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–4 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM}. Use the EPE to get supply current estimates for remaining power supplies.

Table 1–4. Supply Current Specifications for V_{CC_CLKIN} and V_{CCPGM}

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	250	mA
I_{PGM}	V_{CCPGM} current specifications	0	250	mA

I/O Pin Leakage Current

Table 1–5 defines Stratix III I/O Pin leakage current specifications.

Table 1–5. Stratix III I/O Pin Leakage Current *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	-10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	-10	—	10	µA

Notes to Table 1–5:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) 10-µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold Specifications

Table 1–7 shows the Stratix III device family bus hold specifications.

Table 1–6. Bus Hold Parameters (Part 1 of 2)

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2V		1.5V		1.8V		2.5V		3.0V/3.3V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN}>V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN}<V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Low overdrive current	I_{ODL}	$0V<V_{IN}<V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA

DSP Block Specifications

Table 1–21 describes the Stratix III DSP block performance specifications.

Table 1–21. Stratix III DSP Block Performance Specifications *(Note 1)*

Mode	Number of Multipliers	C2 *(5)*	C3	C4	C4L		I3	I4	I4L	Unit
		V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
9×9-bit multiplier (a, c, e, g) *(2)*	1	440	365	315	315	240	345	315	225	MHz
9×9-bit multiplier (b, d, f, h) *(2)*	1	500	410	375	375	270	385	375	250	MHz
12×12-bit multiplier (a, e) *(3)*	1	440	365	315	315	240	345	315	225	MHz
12×12-bit multiplier (b, d, f, h) *(3)*	1	500	410	375	375	270	385	375	250	MHz
18×18-bit multiplier	1	600	495	440	440	320	470	440	300	MHz
36×36-bit multiplier	1	440	365	315	315	220	345	315	205	MHz
Double mode	1	440	365	315	315	220	345	315	205	MHz
18×18-bit multiply adder	2	490	405	345	345	250	380	345	235	MHz
18×18-bit multiply adder	4	490	405	345	345	250	380	345	235	MHz
18×18-bit multiply adder with loop back	2	490	405	345	345	250	380	345	235	MHz
18×18-bit multiply adder with loop back *(4)*	2	390	320	300	240	180	300	300	135	MHz
18×18-bit multiply accumulator	4	475	390	330	330	240	370	330	225	MHz
18×18-bit multiply adder with chainout	4	475	390	330	330	240	370	330	225	MHz
Input Cascade Independent output of four 18×18 bit multiplier	4	550	455	415	415	270	430	415	250	MHz
36-bit shift (32 bit data)	1	475	390	330	330	250	370	330	235	MHz

Notes to Table 1–21:

(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.

(2) The DSP block implements 8 independent 9b × 9b multiplies using a, b, c, d for top DSP half block and e, f, g, h for bottom DSP half block multipliers.

(3) The DSP block implements 6 independent 12b × 12b multiplies using a, b, d for top DSP half block and e, f, h for bottom DSP half block multipliers.

(4) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

(5) The F_{max} for EP3SL200, EP3SE260, and EP3SL340 at C2 Speed Grade is 7% slower than the C2 values shown in the table.

芯片详细信息

Manufacturer Part Number: EP3C80F780C8N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: 29 X 29 MM, 2.60 MM HEIGHT, 1 MM PITCH, LEAD FREE, FBGA-780	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 1.56	Clock Frequency-Max: 472.5 MHz	JESD-30 Code: R-PBGA-B780
JESD-609 Code: e1	Length: 29 mm	Moisture Sensitivity Level: 3	Number of CLBs: 81264
Number of Inputs: 429	Number of Logic Cells: 81264	Number of Outputs: 429	Number of Terminals: 780
Operating Temperature-Max: 85 °C	Organization: 81264 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA780,28X28,40	Package Shape: RECTANGULAR	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 245
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.5 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V	Surface Mount: YES
Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: Tin/Silver/Copper (Sn/Ag/Cu)	Terminal Form: BALL
Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 40	Width: 29 mm

Table 1–53. EP3SL70 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS II	GCLK	t_{su}	-0.759	-0.779	-1.137	-1.243	-1.364	-1.307	-1.592	-1.242	-1.357	-1.306	-1.624	ns
		t_h	0.876	0.911	1.325	1.453	1.596	1.526	1.814	1.461	1.599	1.534	1.844	ns
	GCLK PLL	t_{su}	0.885	0.901	1.451	1.657	1.843	1.743	1.564	1.669	1.859	1.756	1.616	ns
		t_h	-0.638	-0.640	-1.064	-1.217	-1.352	-1.282	-1.097	-1.220	-1.357	-1.287	-1.148	ns
SSTL-18 CLASS I	GCLK	t_{su}	-0.752	-0.773	-1.125	-1.238	-1.364	-1.305	-1.593	-1.238	-1.362	-1.308	-1.628	ns
		t_h	0.869	0.905	1.312	1.445	1.593	1.523	1.810	1.454	1.599	1.535	1.843	ns
	GCLK PLL	t_{su}	0.892	0.907	1.463	1.662	1.843	1.745	1.566	1.673	1.854	1.754	1.615	ns
		t_h	-0.645	-0.646	-1.077	-1.225	-1.355	-1.285	-1.104	-1.227	-1.357	-1.286	-1.152	ns
SSTL-18 CLASS II	GCLK	t_{su}	-0.752	-0.773	-1.125	-1.238	-1.364	-1.305	-1.593	-1.238	-1.362	-1.308	-1.628	ns
		t_h	0.869	0.905	1.312	1.445	1.593	1.523	1.810	1.454	1.599	1.535	1.843	ns
	GCLK PLL	t_{su}	0.892	0.907	1.463	1.662	1.843	1.745	1.566	1.673	1.854	1.754	1.615	ns
		t_h	-0.645	-0.646	-1.077	-1.225	-1.355	-1.285	-1.104	-1.227	-1.357	-1.286	-1.152	ns
SSTL-15 CLASS I	GCLK	t_{su}	-0.740	-0.762	-1.116	-1.227	-1.345	-1.286	-1.574	-1.227	-1.344	-1.290	-1.610	ns
		t_h	0.857	0.894	1.302	1.434	1.574	1.504	1.791	1.443	1.581	1.517	1.825	ns
	GCLK PLL	t_{su}	0.904	0.918	1.472	1.673	1.862	1.764	1.585	1.684	1.872	1.772	1.633	ns
		t_h	-0.657	-0.657	-1.087	-1.236	-1.374	-1.304	-1.123	-1.238	-1.375	-1.304	-1.170	ns
1.8-V HSTL CLASS I	GCLK	t_{su}	-0.740	-0.762	-1.116	-1.227	-1.345	-1.286	-1.574	-1.227	-1.344	-1.290	-1.610	ns
		t_h	0.857	0.894	1.302	1.434	1.574	1.504	1.791	1.443	1.581	1.517	1.825	ns
	GCLK PLL	t_{su}	0.904	0.918	1.472	1.673	1.862	1.764	1.585	1.684	1.872	1.772	1.633	ns
		t_h	-0.657	-0.657	-1.087	-1.236	-1.374	-1.304	-1.123	-1.238	-1.375	-1.304	-1.170	ns
1.8-V HSTL CLASS II	GCLK	t_{su}	-0.752	-0.773	-1.125	-1.238	-1.364	-1.305	-1.593	-1.238	-1.362	-1.308	-1.628	ns
		t_h	0.869	0.905	1.312	1.445	1.593	1.523	1.810	1.454	1.599	1.535	1.843	ns
	GCLK PLL	t_{su}	0.892	0.907	1.463	1.662	1.843	1.745	1.566	1.673	1.854	1.754	1.615	ns
		t_h	-0.645	-0.646	-1.077	-1.225	-1.355	-1.285	-1.104	-1.227	-1.357	-1.286	-1.152	ns
1.5-V HSTL CLASS I	GCLK	t_{su}	-0.752	-0.773	-1.125	-1.238	-1.364	-1.305	-1.593	-1.238	-1.362	-1.308	-1.628	ns
		t_h	0.869	0.905	1.312	1.445	1.593	1.523	1.810	1.454	1.599	1.535	1.843	ns
	GCLK PLL	t_{su}	0.892	0.907	1.463	1.662	1.843	1.745	1.566	1.673	1.854	1.754	1.615	ns
		t_h	-0.645	-0.646	-1.077	-1.225	-1.355	-1.285	-1.104	-1.227	-1.357	-1.286	-1.152	ns
1.5-V HSTL CLASS II	GCLK	t_{su}	-0.740	-0.762	-1.116	-1.227	-1.345	-1.286	-1.574	-1.227	-1.344	-1.290	-1.610	ns
		t_h	0.857	0.894	1.302	1.434	1.574	1.504	1.791	1.443	1.581	1.517	1.825	ns
	GCLK PLL	t_{su}	0.904	0.918	1.472	1.673	1.862	1.764	1.585	1.684	1.872	1.772	1.633	ns
		t_h	-0.657	-0.657	-1.087	-1.236	-1.374	-1.304	-1.123	-1.238	-1.375	-1.304	-1.170	ns
1.2-V HSTL CLASS I	GCLK	t_{su}	-0.740	-0.762	-1.116	-1.227	-1.345	-1.286	-1.574	-1.227	-1.344	-1.290	-1.610	ns
		t_h	0.857	0.894	1.302	1.434	1.574	1.504	1.791	1.443	1.581	1.517	1.825	ns
	GCLK PLL	t_{su}	0.904	0.918	1.472	1.673	1.862	1.764	1.585	1.684	1.872	1.772	1.633	ns
		t_h	-0.657	-0.657	-1.087	-1.236	-1.374	-1.304	-1.123	-1.238	-1.375	-1.304	-1.170	ns

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Cyclone III	☐
系列:	Cyclone III EP3C80	☐
逻辑元件数量:	81264 LE	☐
自适应逻辑模块 - ALM:	-	☐
嵌入式内存:	2.68 Mbit	☐
输入/输出端数量:	429 I/O	☐
工作电源电压:	1.15 V to 1.25 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-780	☐
封装:	Tray	☐
商标:	Intel / Altera	
最大工作频率:	315 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	5079 LAB	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	36	
子类别:	Programmable Logic ICs	
总内存:	2810880 bit	
商标名:	Cyclone III	
零件号别名:	967233	
单位重量:	12 g	