4. Hot Socketing & Power-On Reset

Stratix® II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix II board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix II devices on printed circuit boards (PCBs) that also contain a mixture of 5.0-, 3.3-, 2.5-, 1.8-, 1.5- and 1.2-V devices. With the Stratix II hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix II hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Stratix II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Stratix II Hot-Socketing Specifications

Stratix II devices offer hot socketing capability with all three features listed above without any external components or special design requirements. The hot socketing feature in Stratix II devices allows:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO}, V_{CCPD}, or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

芯片详细信息

Manufacturer Part Number: EP3C80F484I8N	Rohs Code: Yes	Part Life Cycle Code: Contact Manufacturer	Ihs Manufacturer: INTEL CORP
Package Description: BGA, BGA484,22X22,40	Reach Compliance Code: compliant	Manufacturer: Intel Corporation	Risk Rank: 5.58
JESD-30 Code: S-PBGA-B484	JESD-609 Code: e1	Length: 23 mm	Number of Inputs: 295
Number of Logic Cells: 81264	Number of Outputs: 295	Number of Terminals: 484	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA484,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): NOT SPECIFIED	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.4 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V
Surface Mount: YES	Technology: CMOS	Terminal Finish: TIN SILVER COPPER	Terminal Form: BALL
Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): NOT SPECIFIED	Width: 23 mm

For more information on JTAG, see the following documents:

- The *IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing for Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2*
- Jam Programming & Test Language Specification

SignalTap II Embedded Logic Analyzer

Stratix II devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II architecture are configured with CMOS SRAM elements. Altera® FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (e.g., a MAX® II device or microprocessor). Stratix II devices can be configured using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and AES technology, provides a mechanism to protect your designs. The decompression feature allows Stratix II FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of your Stratix II designs. For more information, see "Configuration Schemes" on page 3–7.

The PLL_ENA pin and the configuration input pins (Table 3–4) have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The VCCSEL input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by $V_{CCPD,}$ while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}. Table 3–4 shows the pins affected by VCCSEL.

Table 3–4. Pins Affected by the Voltage Level at VCCSEL

Pin	VCCSEL = LOW (connected to GND)	VCCSEL = HIGH (connected to V_{CCPD})
nSTATUS (when used as an input)	3.3/2.5-V input buffer is selected. Input buffer is powered by V_{CCPD}.	1.8/1.5-V input buffer is selected. Input buffer is powered by V_{CCIO} of the I/O bank.
nCONFIG		
CONF_DONE (when used as an input)		
DATA[7..0]		
nCE		
DCLK (when used as an input)		
CS		
nWS		
nRS		
nCS		
CLKUSR		
DEV_OE		
DEV_CLRn		
RUnLU		
PLL_ENA		

VCCSEL is sampled during power-up. Therefore, the VCCSEL setting cannot change on the fly or during a reconfiguration. The VCCSEL input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high VCCSEL connection selects the 1.8-V/1.5-V input buffer, and a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX® II/microprocessor.

If you need to support configuration input voltages of 3.3 V/2.5 V, you should set the VCCSEL to a logic low; you can set the V_{CCIO} of the I/O bank that contains the configuration inputs to any supported voltage. If

XC2V3000-5CS144I	2001+	BGA	2315
XC2V3000-5CS144C	2001+	BGA	2315
XC2V3000-5CFF1152	2001+	BGA	2315
XC2V3000-5BGG728I	2001+	BGA728	2315
XC2V3000-5BGG728C	2001+	BGA728	2315
XC2V3000-5BG957C	2001+	BGA	2315
XC2V3000-5BG782	2001+	BGA	2315
XC2V3000-5BG728IES	2001+	BGA	2315
XC2V3000-5BG728I	2001+	BGA728	2315
XC2V3000-5BG728C	2001+	BGA728	2315
XC2V30005BG728C	2001+	原厂原封	2315
XC2V3000-5BG728	2001+	BGA	2315
XC2V3000-5BG728	2001+	BGA	2315
XC2V3000-5BFG957I	2001+	BGA	2315
XC2V3000-5BFG957C	2001+	BGA	2315
XC2V3000-5BF957I	2001+	BGA957	2315
XC2V3000-5BF957I	2001+	BGA	2315
XC2V3000-5BF957C-ES	2001+	BGA	2315
XC2V3000-5BF957C	2001+	BGA	2315
XC2V30005BF957C	2001+	BGA	2315
XC2V3000-5BF957	2001+	NA	2315
XC2V3000-4I/FG676	2001+	BGA	2315
XC2V3000-4FGG676I	2001+	BGA	2315
XC2V3000-4FGG676C	2001+	SMD	2315
XC2V3000-4FG728C	2001+	原厂原封	2315
XC2V3000-4FG676I0958	2001+	BGA	2315
XC2V3000-4FG676I	2001+	BGA	2315
XC2V3000-4FG676-I	2001+	BGA	2315
XC2V3000-4FG676I	2001+	BGA	2315
XC2V30004FG676I	2001+	BGA	2315
XC2V3000-4FG676C-ES	2001+	BGA	2315
XC2V3000-4FG676CE-S	2001+	BGA	2315
XC2V3000-4FG676C	2001+	BGA	2315
XC2V3000-4FG676	2001+	BGA676	2315
xc2v3000-4fg676	2001+	BGA2323	2315
XC2V3000-4FG456I	2001+	BGA	2315
XC2V3000-4FG456C	2001+	BGA	2315
XC2V3000-4FG256I	2001+	BGA	2315
XC2V3000-4FG256C	2001+	BGA	2315
XC2V3000-4FFR1152	2001+	BGA	2315
XC2V3000-4FFG1152I	2001+	BGA	2315