MLABs support byte-enable via emulation. There will be increased logic utilization when the byte-enables are emulated.

The default value for the byte-enable signals is high (enabled), in which case writing is controlled only by the write enable signals. The byte-enable registers have no clear port. When using parity bits on the M9K and M144K blocks, the byte-enable controls all nine bits (eight bits of data plus one parity bit). When using parity bits on the MLAB, the byte-enable controls all 10 bits in the widest mode.

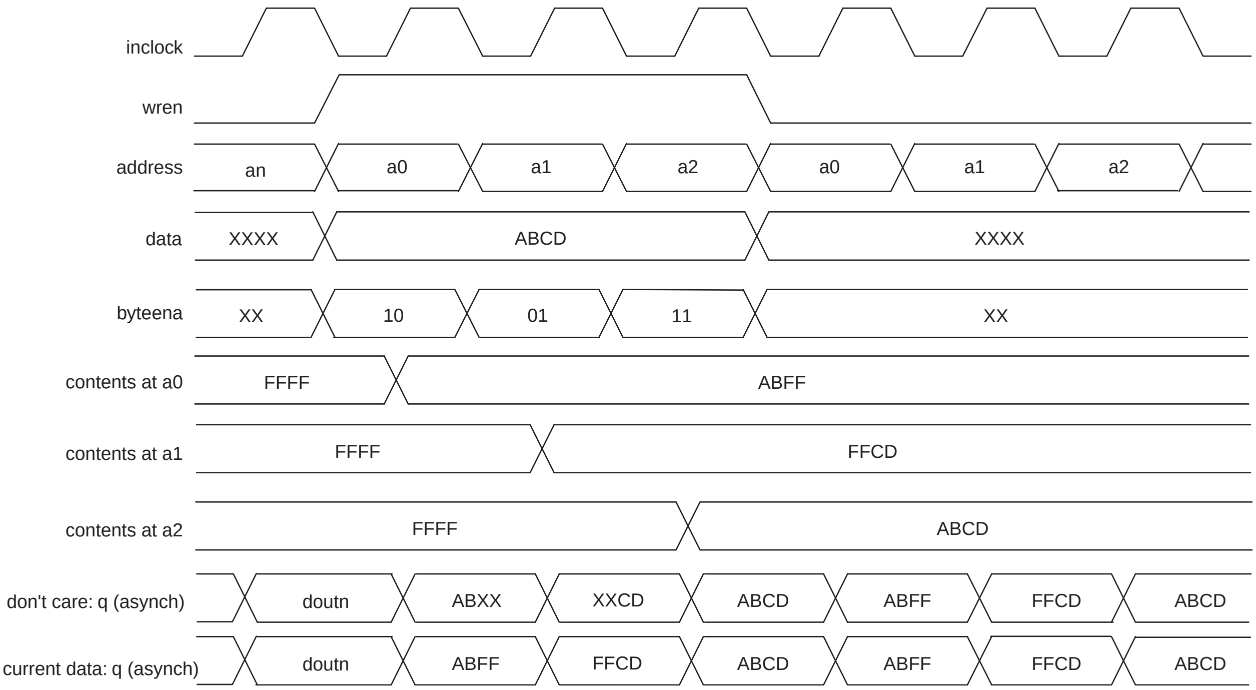
Byte-enables operate in a one-hot fashion, with the LSB of the `byteena` signal corresponding to the least significant byte of the data bus. For example, if you are using a RAM block in ×18 mode, with `byteena = 01`, `data[8..0]` is enabled and `data[17..9]` is disabled. Similarly, if `byteena = 11`, both `data[8..0]` and `data[17..9]` are enabled. Byte-enables are active high.

You cannot use the byte-enable feature when using the ECC feature on M144K blocks.

Figure 4–1 shows how the write enable (`wren`) and byte-enable (`byteena`) signals control the operations of the M9K and M144K.

When a byte-enable bit is de-asserted during a write cycle, the corresponding data byte output can appear as either a "don't care" value or the current data at that location. The output value for the masked byte is controllable via the Quartus II software. When a byte-enable bit is asserted during a write cycle, the corresponding data byte output also depends on the setting chosen in the Quartus II software.

**Figure 4–1.** Stratix III Byte-Enable Functional Waveform for M9K and M144K



In simple dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output a don't care value or old data. To choose the desired behavior, set the read-during-write behavior to either don't care or old data in the RAM MegaWizard Plug-In Manager in the Quartus II software. See "Read During Write" on page 4–21 for more details about this behavior.

MLABs only support a write-enable signal. Read-during-write behavior for the MLABs can be either don't care, new data, or old data. The available choices depend on the configuration of the MLAB.

Figure 4–13 shows the timing waveforms for read and write operations in simple dual-port mode with unregistered outputs in M9K and M144K. Registering the RAM's outputs would simply delay the q output by one clock cycle in M9k and M144K.

**Figure 4–13.** Stratix III Simple Dual-Port Timing Waveforms for M9K and M144K

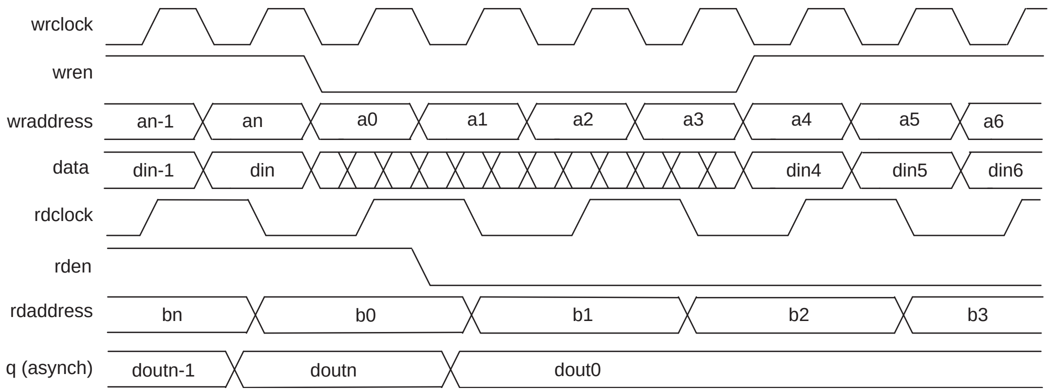
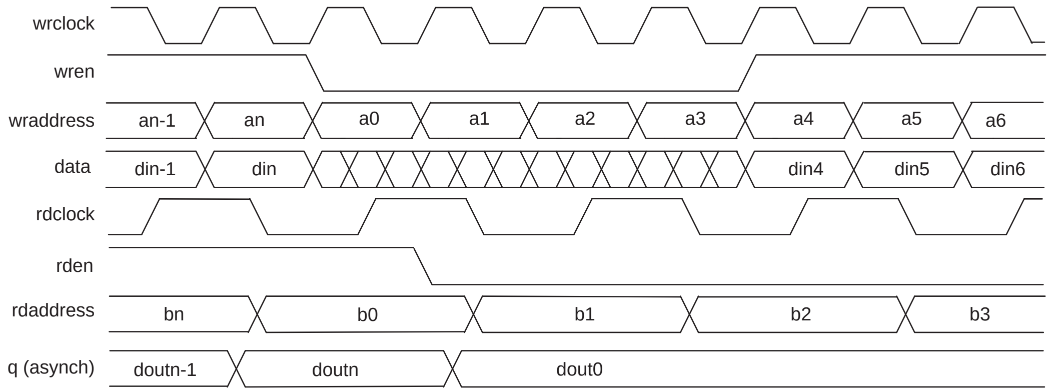
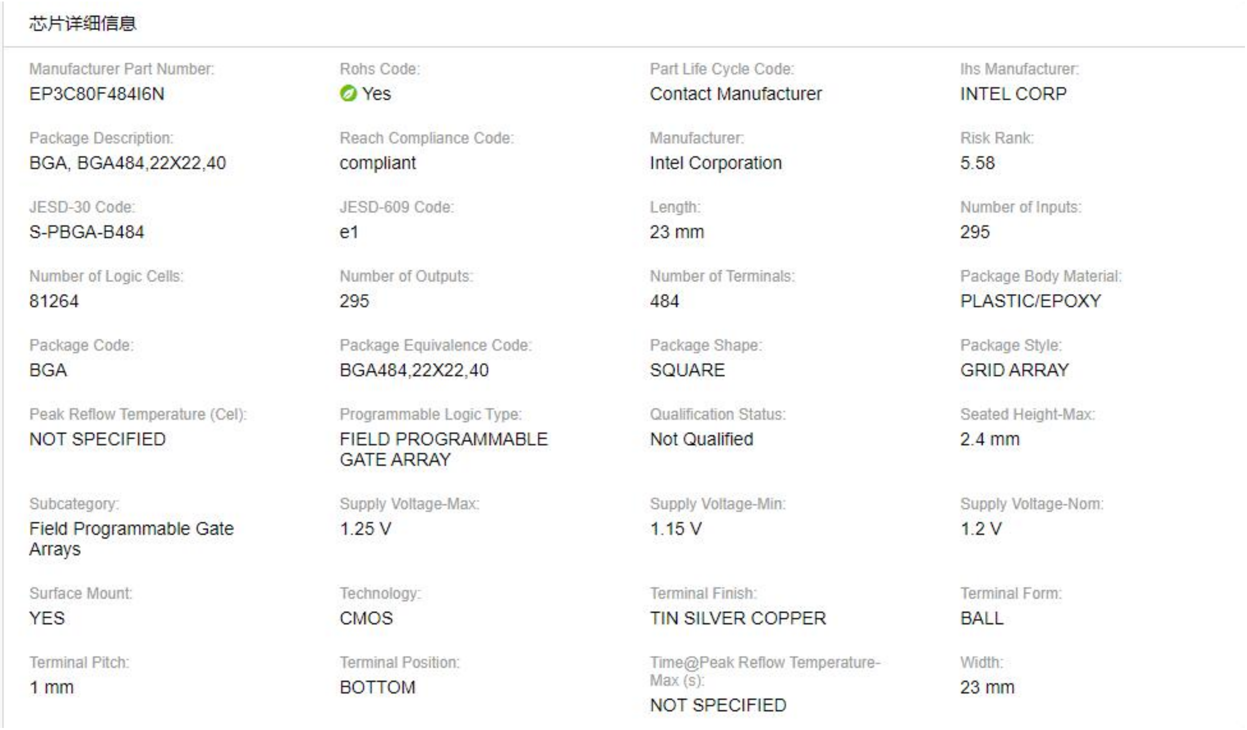


Figure 4–14 shows the timing waveforms for read and write operations in simple dual-port mode with unregistered outputs in MLABs. In MLABs, the write operation is triggered by the falling clock edges.

**Figure 4–14.** Stratix III Simple Dual-Port Timing Waveforms for MLABs





芯片详细信息

| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>EP3C80F484I6N | Rohs Code:<br>✓ Yes | Part Life Cycle Code:<br>Contact Manufacturer | Ihs Manufacturer:<br>INTEL CORP |
| Package Description:<br>BGA, BGA484,22X22,40 | Reach Compliance Code:<br>compliant | Manufacturer:<br>Intel Corporation | Risk Rank:<br>5.58 |
| JESD-30 Code:<br>S-PBGA-B484 | JESD-609 Code:<br>e1 | Length:<br>23 mm | Number of Inputs:<br>295 |
| Number of Logic Cells:<br>81264 | Number of Outputs:<br>295 | Number of Terminals:<br>484 | Package Body Material:<br>PLASTIC/EPOXY |
| Package Code:<br>BGA | Package Equivalence Code:<br>BGA484,22X22,40 | Package Shape:<br>SQUARE | Package Style:<br>GRID ARRAY |
| Peak Reflow Temperature (Cel):<br>NOT SPECIFIED | Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY | Qualification Status:<br>Not Qualified | Seated Height-Max:<br>2.4 mm |
| Subcategory:<br>Field Programmable Gate Arrays | Supply Voltage-Max:<br>1.25 V | Supply Voltage-Min:<br>1.15 V | Supply Voltage-Nom:<br>1.2 V |
| Surface Mount:<br>YES | Technology:<br>CMOS | Terminal Finish:<br>TIN SILVER COPPER | Terminal Form:<br>BALL |
| Terminal Pitch:<br>1 mm | Terminal Position:<br>BOTTOM | Time@Peak Reflow Temperature-Max (s):<br>NOT SPECIFIED | Width:<br>23 mm |

Shift registers are useful in DSP functions such as FIR filters. When implementing 18 × 18 or smaller width multipliers, you do not need external logic to create the shift register chain because the input shift registers are internal to the DSP block. This implementation significantly reduces the logical element (LE) resources required, avoids routing congestion, and results in predictable timing.

The first multiplier in every half DSP block (top- and bottom-half) in Stratix III devices has a multiplexer for the first multiplier B-input (lower-leg input) register to select between general routing and loopback, as shown in Figure 5–6. In loopback mode, the most significant 18-bit registered outputs are connected as feedback to the multiplier input of the first top multiplier in each half DSP block. Loopback modes are used by recursive filters where the previous output is needed to compute the current output.

The loopback mode is described in detail in "Two-Multiplier Adder Sum Mode" on page 5–21.

Table 5–3 lists the input register modes for the DSP block.

**Table 5–3.** Input Register Modes

| Register Input Mode *(1)* | 9 × 9 | 12 × 12 | 18 × 18 | 36 × 36 | Double |
|---|---|---|---|---|---|
| Parallel input | ✓ | ✓ | ✓ | ✓ | ✓ |
| Shift register input *(2)* | — | — | ✓ | — | — |
| Loopback input *(3)* | — | — | ✓ | — | — |

**Notes to Table 5–3:**

(1) The multiplier operand input wordlengths are statically configured at compile time.

(2) Available only on the A-operand.

(3) Only one loopback input is allowed per Half-Block. See Figure 5–15 for details.

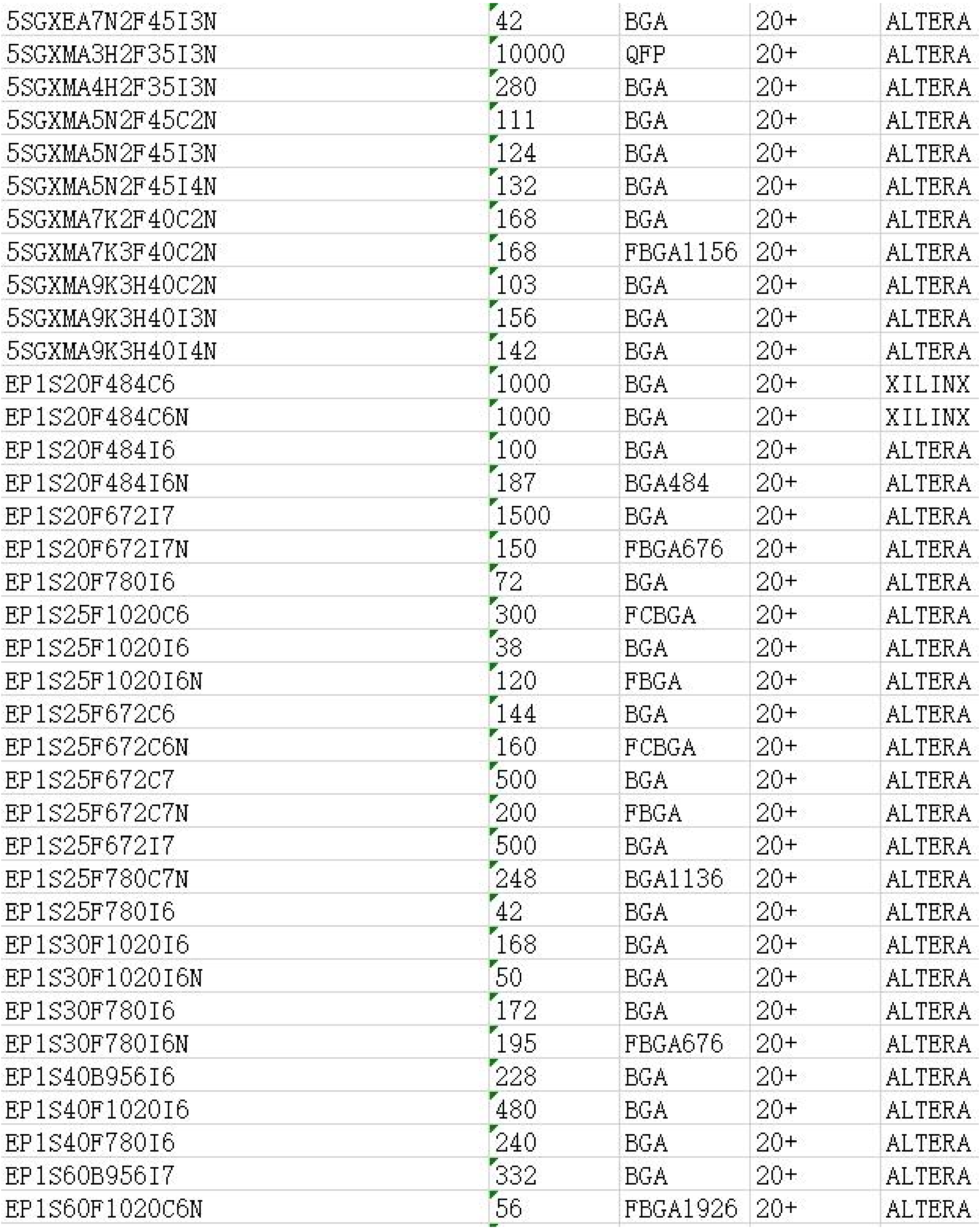
## Multiplier and First-Stage Adder

The multiplier stage natively supports 9 × 9, 12 × 12, 18 × 18, or 36 × 36 multipliers. Other wordlengths are padded up to the nearest appropriate native wordlength; for example, 16 × 16 would be padded up to use 18 × 18. Refer to "Independent Multiplier Modes" on page 5–15 for more details. Depending on the data width of the multiplier, a single DSP block can perform many multiplications in parallel.

Each multiplier operand can be a unique signed or unsigned number. Two dynamic signals, `signa` and `signb`, control the representation of each operand, respectively. A `logic 1` value on the `signa/signb` signal indicates that `data A/data B` is a signed number; a `logic 0` value indicates an unsigned number. Table 5–4 lists the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

**Table 5–4.** Multiplier Sign Representation

| Data A<br>(signa Value) | Data B<br>(signb Value) | Result |
|---|---|---|
| Unsigned (`logic 0`) | Unsigned (`logic 0`) | Unsigned |
| Unsigned (`logic 0`) | Signed (`logic 1`) | Signed |
| Signed (`logic 1`) | Unsigned (`logic 0`) | Signed |
| Signed (`logic 1`) | Signed (`logic 1`) | Signed |



| | | | | |
|---|---|---|---|---|
| 5SGXEA7N2F45I3N | 42 | BGA | 20+ | ALTERA |
| 5SGXMA3H2F35I3N | 10000 | QFP | 20+ | ALTERA |
| 5SGXMA4H2F35I3N | 280 | BGA | 20+ | ALTERA |
| 5SGXMA5N2F45C2N | 111 | BGA | 20+ | ALTERA |
| 5SGXMA5N2F45I3N | 124 | BGA | 20+ | ALTERA |
| 5SGXMA5N2F45I4N | 132 | BGA | 20+ | ALTERA |
| 5SGXMA7K2F40C2N | 168 | BGA | 20+ | ALTERA |
| 5SGXMA7K3F40C2N | 168 | FBGA1156 | 20+ | ALTERA |
| 5SGXMA9K3H40C2N | 103 | BGA | 20+ | ALTERA |
| 5SGXMA9K3H40I3N | 156 | BGA | 20+ | ALTERA |
| 5SGXMA9K3H40I4N | 142 | BGA | 20+ | ALTERA |
| EP1S20F484C6 | 1000 | BGA | 20+ | XILINX |
| EP1S20F484C6N | 1000 | BGA | 20+ | XILINX |
| EP1S20F484I6 | 100 | BGA | 20+ | ALTERA |
| EP1S20F484I6N | 187 | BGA484 | 20+ | ALTERA |
| EP1S20F672I7 | 1500 | BGA | 20+ | ALTERA |
| EP1S20F672I7N | 150 | FBGA676 | 20+ | ALTERA |
| EP1S20F780I6 | 72 | BGA | 20+ | ALTERA |
| EP1S25F1020C6 | 300 | FCBGA | 20+ | ALTERA |
| EP1S25F1020I6 | 38 | BGA | 20+ | ALTERA |
| EP1S25F1020I6N | 120 | FBGA | 20+ | ALTERA |
| EP1S25F672C6 | 144 | BGA | 20+ | ALTERA |
| EP1S25F672C6N | 160 | FCBGA | 20+ | ALTERA |
| EP1S25F672C7 | 500 | BGA | 20+ | ALTERA |
| EP1S25F672C7N | 200 | FBGA | 20+ | ALTERA |
| EP1S25F672I7 | 500 | BGA | 20+ | ALTERA |
| EP1S25F780C7N | 248 | BGA1136 | 20+ | ALTERA |
| EP1S25F780I6 | 42 | BGA | 20+ | ALTERA |
| EP1S30F1020I6 | 168 | BGA | 20+ | ALTERA |
| EP1S30F1020I6N | 50 | BGA | 20+ | ALTERA |
| EP1S30F780I6 | 172 | BGA | 20+ | ALTERA |
| EP1S30F780I6N | 195 | FBGA676 | 20+ | ALTERA |
| EP1S40B956I6 | 228 | BGA | 20+ | ALTERA |
| EP1S40F1020I6 | 480 | BGA | 20+ | ALTERA |
| EP1S40F780I6 | 240 | BGA | 20+ | ALTERA |
| EP1S60B956I7 | 332 | BGA | 20+ | ALTERA |
| EP1S60F1020C6N | 56 | FBGA1926 | 20+ | ALTERA |