Table 1–25. True & Emulated LVDS Specifications *(Note 1)*, *(2)* (Part 3 of 3)

Symbol	Conditions	C2			C3, I3			C4, I4			C4L, I4L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Non DPA Mode														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

Notes to Table 1–25:

(1) When J = 3 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum and maximum specification is dependent on the clock source (PLL and clock pin, for example) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) The $t_{xJitter}$ specification is for true LVDS IO standard only.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing the link timing closure analysis. You should consider the board skew margin, transmitter delay margin as well as the receiver sampling margin to determine the maximum data rate supported.

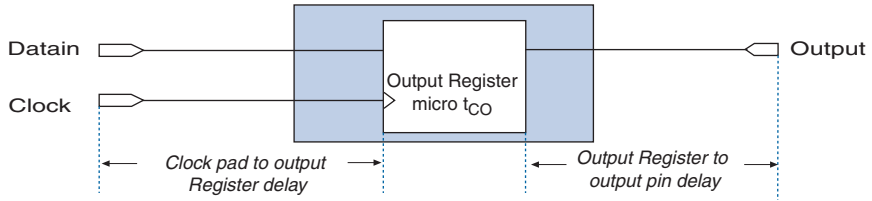
(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

Table 1–26. Stratix III DPA Lock Time Specifications *(Note 1)*, *(2)*, *(3)* (Part 1 of 2)

Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetitions per 256 data transition *(4)*	Condition *(5)*	Min	Typ	Max
SPI-4	0000000000 1111111111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3×256 data transitions + 2×96 slow clock cycles *(6)*	—	—
Parallel Rapid I/O	00001111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3×256 data transitions + 2×96 slow clock cycles *(6)*	—	—
	10010000	4	64	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3×256 data transitions + 2×96 slow clock cycles *(6)*	—	—

Figure 1–5. Output Register Clock to Output Timing Diagram

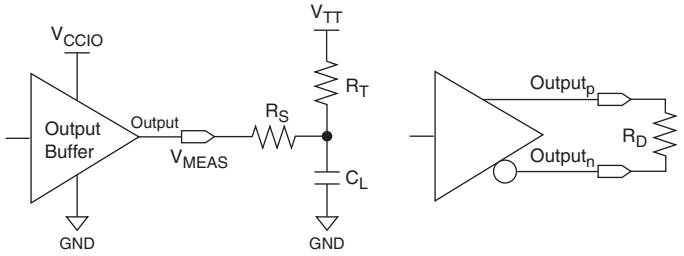


Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 1–39.
2. Record the time to V_{MEAS} at the far end of the PCB trace.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} at the far end of the PCB trace.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 1–39 using the above equation. Figure 1–6 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 1–6. Output Delay Timing Reporting Setup Modeled by Quartus II Software for Single-Ended Outputs and Dedicated Differential Outputs *(Note 1)*



Note to Figure 1–6:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

EP1S30F780I6	172	BGA	20+	ALTERA
EP1S30F780I6N	195	FBGA676	20+	ALTERA
EP1S40B956I6	228	BGA	20+	ALTERA
EP1S40F1020I6	480	BGA	20+	ALTERA
EP1S40F780I6	240	BGA	20+	ALTERA
EP1S60B956I7	332	BGA	20+	ALTERA
EP1S60F1020C6N	56	FBGA1926	20+	ALTERA
EP1S60F1020C7N	20	FBGA1157	20+	ALTERA
EP1S80F1020C5N	143	BGA1759	20+	ALTERA
EP1S80F1020I6N	453	FCBGA1156	20+	ALTERA
EP1SGX25DF672C7N	20	BGA	20+	ALTERA
EP1SGX40DF1020C6N	386	BGA	20+	ALTERA
EP1SGX40GF1020I6	5	BGA	20+	ALTERA
EP2A15F672C7N	269	BGA1156	20+	ALTERA
EP2AGX125EF29C4N	300	BGA	20+	ALTERA
EP2AGX125EF29C4N	120	BGA	20+	Intel/Altera
EP2AGX125EF29C5N	215	BGA1517	20+	ALTERA
EP2AGX125EF29C6G	88	BGA	20+	ALTERA
EP2AGX125EF29I3N	680	BGA	20+	Intel/Altera
EP2AGX125EF29I3N	710	LSSN	20+	ALTERA
EP2AGX125EF35C5N	192	BGA	20+	ALTERA
EP2AGX125EF35I3N	280	BGA	20+	ALTERA
EP2AGX125EF35I5N	120	BGA	20+	ALTERA
EP2AGX190EF29C4N	130	BGA	20+	ALTERA
EP2AGX190EF29C5N	117	BGA	20+	ALTERA
EP2AGX190EF29C6G	172	BGA	20+	XILINX
EP2AGX190EF29C6N	461	BGA	20+	ALTERA
EP2AGX190EF29I3N	96	BGA	20+	ALTERA
EP2AGX190EF29I5N	55	BGA	20+	Intel/Altera
EP2AGX190FF35C5N	500	BGA	20+	ALTERA
EP2AGX190FF35C6N	30	BGA	20+	ALTERA
EP2AGX190FF35I3N	400	FBGA665	20+	ALTERA
EP2AGX190FF35I5N	1080	TQFP	20+	ALTERA
EP2AGX260EF29C5N	12	BGA	20+	ALTERA
EP2AGX260EF29C6N	25	BGA	20+	Intel/Altera
EP2AGX260EF29I3N	25	BGA	20+	Intel/Altera
EP2AGX260FF35C4N	2000	SOP	20+	ALTERA

Table 1–45. EP3SL50 Column Pins output Timing Parameters (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	2mA	GCLK	t_{co}	3.188	3.431	4.876	5.290	5.813	5.680	5.908	5.427	5.951	5.821	5.996	ns
		GCLK PLL	t_{co}	1.754	1.959	2.573	2.707	2.956	2.961	2.902	2.833	3.081	3.085	2.904	ns
	4mA	GCLK	t_{co}	3.090	3.320	4.724	5.132	5.652	5.519	5.747	5.268	5.785	5.655	5.830	ns
		GCLK PLL	t_{co}	1.656	1.848	2.421	2.548	2.804	2.809	2.750	2.673	2.915	2.919	2.738	ns
	6mA	GCLK	t_{co}	3.008	3.233	4.597	4.994	5.508	5.375	5.603	5.124	5.638	5.508	5.683	ns
		GCLK PLL	t_{co}	1.573	1.760	2.293	2.409	2.663	2.668	2.609	2.527	2.766	2.770	2.589	ns
	8mA	GCLK	t_{co}	2.983	3.200	4.536	4.928	5.433	5.300	5.528	5.053	5.557	5.427	5.602	ns
		GCLK PLL	t_{co}	1.548	1.727	2.233	2.344	2.584	2.589	2.530	2.457	2.686	2.690	2.509	ns
	10mA	GCLK	t_{co}	2.912	3.136	4.448	4.834	5.334	5.201	5.429	4.956	5.456	5.326	5.501	ns
		GCLK PLL	t_{co}	1.477	1.663	2.145	2.250	2.502	2.507	2.448	2.360	2.585	2.589	2.408	ns
	12mA	GCLK	t_{co}	2.907	3.126	4.442	4.828	5.327	5.194	5.422	4.949	5.449	5.319	5.494	ns
		GCLK PLL	t_{co}	1.472	1.654	2.139	2.244	2.496	2.501	2.442	2.353	2.578	2.582	2.401	ns
1.5 V	2mA	GCLK	t_{co}	3.129	3.398	4.814	5.217	5.741	5.608	5.836	5.357	5.884	5.754	5.929	ns
		GCLK PLL	t_{co}	1.694	1.926	2.512	2.635	2.895	2.900	2.841	2.762	3.014	3.018	2.837	ns
	4mA	GCLK	t_{co}	2.997	3.217	4.571	4.963	5.470	5.337	5.565	5.089	5.598	5.468	5.643	ns
		GCLK PLL	t_{co}	1.562	1.744	2.267	2.378	2.626	2.631	2.572	2.493	2.726	2.730	2.549	ns
	6mA	GCLK	t_{co}	2.953	3.180	4.490	4.883	5.390	5.257	5.485	5.009	5.515	5.385	5.560	ns
		GCLK PLL	t_{co}	1.518	1.707	2.187	2.299	2.564	2.569	2.510	2.413	2.643	2.647	2.466	ns
	8mA	GCLK	t_{co}	2.941	3.174	4.484	4.876	5.381	5.248	5.476	5.002	5.507	5.377	5.552	ns
		GCLK PLL	t_{co}	1.507	1.701	2.181	2.291	2.557	2.562	2.503	2.406	2.635	2.639	2.458	ns
	10mA	GCLK	t_{co}	2.906	3.123	4.436	4.822	5.320	5.187	5.415	4.943	5.442	5.312	5.487	ns
		GCLK PLL	t_{co}	1.471	1.651	2.133	2.238	2.498	2.503	2.444	2.347	2.571	2.575	2.394	ns
	12mA	GCLK	t_{co}	2.902	3.116	4.416	4.801	5.300	5.167	5.395	4.922	5.421	5.291	5.466	ns
		GCLK PLL	t_{co}	1.467	1.644	2.112	2.216	2.495	2.500	2.441	2.326	2.549	2.553	2.372	ns

EP2AGX260FF35C4N	2000	SOP	20+	ALTERA
EP2AGX260FF35C6N	110	FBGA	20+	ALTERA
EP2AGX260FF35I3N	263	FCBGA676	20+	ALTERA
EP2AGX260FF35I5N	165	BGA	20+	ALTERA
EP2AGX45CU17C4N	50	BGA	20+	ALTERA
EP2AGX45CU17I3G	50	BGA	20+	ALTERA
EP2AGX45DF25I3N	100	FBGA1156	20+	ALTERA
EP2AGX45DF29C5N	293	FCBGA1152	20+	ALTERA
EP2AGX45DF29I3N	167	FBGA1156	20+	ALTERA
EP2AGX65DF25C6N	263	FCBGA1738	20+	ALTERA
EP2AGX65DF25I3N	500	BGA900	20+	ALTERA
EP2AGX65DF25I5N	190	BGA2397	20+	XILINX
EP2AGX65DF25I5N	120	FBGA	20+	ALTERA
EP2AGX65DF29C4N	120	FBGA	20+	ALTERA
EP2AGX65DF29C5N	45	BGA	20+	ALTERA
EP2AGX65DF29C6N	116	FCBGA1517	20+	ALTERA
EP2AGX65DF29I3N	60	BGA	20+	Intel/Altera
EP2AGX65DF29I3N	133	FCBGA1517	20+	ALTERA
EP2AGX65DF29I5N	172	BGA	20+	ALTERA
EP2AGX95DF25C4N	200	FCBGA	20+	ALTERA
EP2AGX95DF25C6N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I5N	58	FPBGA102C	20+	ALTERA
EP2AGX95EF29C4N	1080	BGA	20+	ALTERA
EP2AGX95EF29C5N	50	BGA	20+	Intel/Altera
EP2AGX95EF29C5N	50	BGA	20+	ALTERA
EP2AGX95EF29C6N	15	BGA	20+	ALTERA
EP2AGX95EF29I3N	72	FBGA1156	20+	ALTERA
EP2AGX95EF35C6N	455	FBGA1152	20+	ALTERA
EP2AGX95EF35I3N	400	DIP	20+	ALTERA
EP2AGX95EF35I5N	426	BGA1152	20+	ALTERA
EP2AGZ300FF35I3N	500	TO220-7	20+	ALTERA
EP2AGZ300FH29I3N	4000	DIP16	20+	ALTERA
EP2AGZ300HF40I3N	1400	SOP	20+	ALTERA
EP2AGZ300HF40I4N	1500	PWRSO-10	20+	ALTERA
EP2AGZ350FF35I3N	50	BGA	20+	ALTERA