SGMII GTX Transceiver Clock Generation

[Figure 1-2, callout 16]

An Integrated Circuit Systems ICS844021I chip (U2) generates a high-quality, low-jitter, 125 MHz LVDS clock from a 25 MHz crystal (X3). This clock is sent to FPGA U1, Bank 113 GTX transceiver (clock pins AH8 (P) and AH7 (N)) driving the SGMII interface. Series AC coupling capacitors are present to allow the clock input of the FPGA to set the common mode voltage. Figure 1-17 shows the Ethernet SGMII clock source.

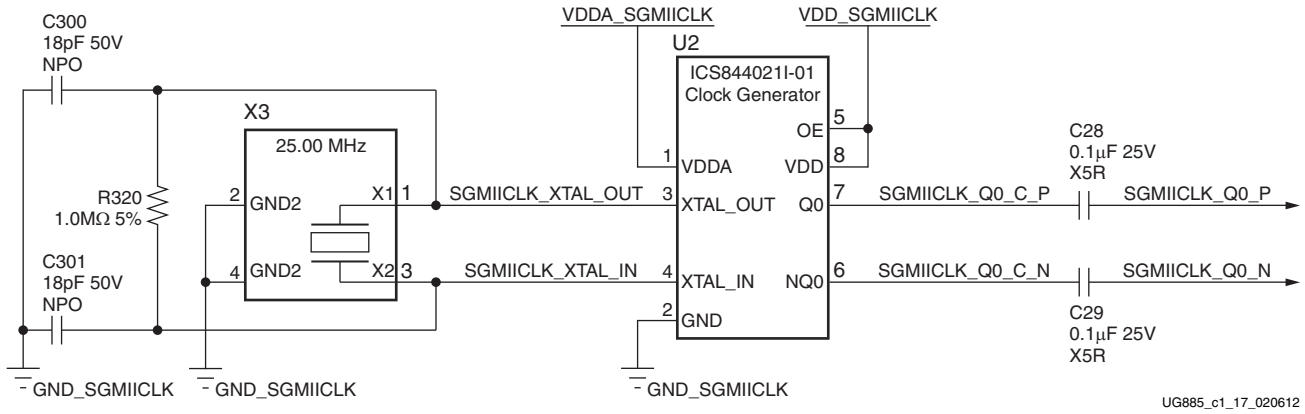

Figure 1-17: **Ethernet 125 MHz SGMII GTX Clock**

References

Details about the tri-mode Ethernet MAC core are provided in *LogiCORE IP Tri-Mode Ethernet MAC Product Guide for Vivado Design Suite* (PG051) [Ref 9] and in the *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide* (UG138) [Ref 13].

The product brief for the Marvell 88E1111 Alaska Gigabit Ethernet Transceiver can be found at the Marvell website [Ref 21].

The data sheet can be obtained under NDA with Marvell. Contact information is at the Marvell website [Ref 21].

For more information about the ICS844021 device, go to the Integrated Device Technology website [Ref 22] and search for part number **ICS844021**.

USB-to-UART Bridge

[Figure 1-2, callout 17]

The VC707 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U44) which allows a connection to a host computer with a USB port. The USB cable is supplied in the VC707 Evaluation Kit (Type-A end to host computer, Type mini-B end to VC707 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VC707 board.

Xilinx UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using four signal pins: Transmit (TX), Receive (RX), Request to Send (RTS), and Clear to Send (CTS).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm) that runs on the host computer. The VCP device

drivers must be installed on the host PC prior to establishing communications with the VC707 board.

The USB Connector Pin Assignments and Signal Definitions between J17 and U44 are listed in Table 1-19.

Table 1-19: **USB Connector J17 Pin Assignments and Signal Definitions**

USB Connector (J17)		Net Name	Description	CP2103GM (U44)	
Pin	Name			Pin	Name
1	VBUS	USB_UART_VBUS	+5V VBUS Powered	7	REGIN
				8	VBUS
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	4	D –
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	3	D +
4	GND	USB_UART_GND	Signal ground	2	GND1
				29	CNR_GND

Table 1-20 shows the USB connections between the FPGA and the UART.

Table 1-20: **FPGA to UART Connections**

FPGA (U1)				Schematic Net Name	CP2013 Device (U12)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AR34	RTS	Output	LVCMOS18	USB_CTS	22	CTS	Input
AT32	CTS	Input	LVCMOS18	USB_RTS	23	RTS	Output
AU36	TX	Output	LVCMOS18	USB_RX	24	RXD	Input
AU33	RX	Input	LVCMOS18	USB_TX	25	TXD	Output

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP drivers [Ref 20].

HDMI Video Output

[Figure 1-2, callout 18]

The VC707 board provides a High-Definition Multimedia Interface (HDMI™) video output using the Analog Devices ADV7511KSTZ-P HDMI transmitter (U48). The HDMI output is provided on a Molex 500254-1927 HDMI type-A connector (P2). The ADV7511 is wired to support 1080P 60 Hz YCbCr and RGB video modes through 36-bit input data mapping.

The VC707 board supports the following HDMI device interfaces:

- 36 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out Pin to FPGA
- I^2C
- SPDIF

Table 1-27: **J35 VITA 57.1 FMC HPC Connections *(Cont'd)***

J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin	J35 FMC 1 HPC Pin	Schematic Net Name	I/O Standard	U1 FPGA Pin
C2	FMC1_HPC_DP0_C2M_P	(1)	E2	D1	PWRCTL1_VCC4B_PG		AL32
C3	FMC1_HPC_DP0_C2M_N	(1)	E1	D4	FMC1_HPC_GBTCLK0_M2C_P	(1)	A10
C6	FMC1_HPC_DP0_M2C_P	(1)	D8	D5	FMC1_HPC_GBTCLK0_M2C_N	(1)	A9
C7	FMC1_HPC_DP0_M2C_N	(1)	D7	D8	FMC1_HPC_LA01_CC_P	LVCMOS18	J40
C10	FMC1_HPC_LA06_P	LVCMOS18	K42	D9	FMC1_HPC_LA01_CC_N	LVCMOS18	J41
C11	FMC1_HPC_LA06_N	LVCMOS18	J42	D11	FMC1_HPC_LA05_P	LVCMOS18	M41
C14	FMC1_HPC_LA10_P	LVCMOS18	N38	D12	FMC1_HPC_LA05_N	LVCMOS18	L41
C15	FMC1_HPC_LA10_N	LVCMOS18	M39	D14	FMC1_HPC_LA09_P	LVCMOS18	R42
C18	FMC1_HPC_LA14_P	LVCMOS18	N39	D15	FMC1_HPC_LA09_N	LVCMOS18	P42
C19	FMC1_HPC_LA14_N	LVCMOS18	N40	D17	FMC1_HPC_LA13_P	LVCMOS18	H39
C22	FMC1_HPC_LA18_CC_P	LVCMOS18	M32	D18	FMC1_HPC_LA13_N	LVCMOS18	G39
C23	FMC1_HPC_LA18_CC_N	LVCMOS18	L32	D20	FMC1_HPC_LA17_CC_P	LVCMOS18	L31
C26	FMC1_HPC_LA27_P	LVCMOS18	J31	D21	FMC1_HPC_LA17_CC_N	LVCMOS18	K32
C27	FMC1_HPC_LA27_N	LVCMOS18	H31	D23	FMC1_HPC_LA23_P	LVCMOS18	P30
C30	FMC1_HPC_IIC_SCL		U52.4	D24	FMC1_HPC_LA23_N	LVCMOS18	N31
C31	FMC1_HPC_IIC_SDA		U52.3	D26	FMC1_HPC_LA26_P	LVCMOS18	J30
C34	GA0 = 0 = GND			D27	FMC1_HPC_LA26_N	LVCMOS18	H30
C35	VCC12_P			D29	FMC1_HPC_TCK_BUF		U19.14
C37	VCC12_P			D30	FMC_TDI_BUF		U19.18
C39	VCC3V3			D31	FMC1_TDO_FMC2_TDI		U27.2
				D32	VCC3V3		
				D33	FMC1_HPC_TMS_BUF		U19.17
				D34	NC		
				D35	GA1 = 0 = GND		
				D36	VCC3V3		
				D38	VCC3V3		
				D40	VCC3V3		

XC3030ATM-7PC44C	2001+	PLCC44	2315
XC3030ATM-7CPC84	2001+	PLCC	2315
XC3030ATM-7CPC68	2001+	PLCC	2315
XC3030ATM-70	2001+	PLCC-84	2315
XC3030ATM-7/PC84C	2001+	PLCC	2315
XC3030ATM-7	2001+	PLCC	2315
XC3030ATM-6C	2001+	PLCC-68	2315
XC3030ATM	2001+	TQFP	2315
XC3030APQ100C-7	2001+	QFP	2315
XC3030A-PQ100BKJ	2001+	QFP	2315
XC3030APQ100BKJ	2001+	QFP	2315
XC3030APQ100BK	2001+	QFP	2315
XC3030APQ100-7C	2001+	BGA	2315
XC3030APQ100-6C	2001+	BGA	2315
XC3030A-PQ100	2001+	QFP	2315
XC3030APQ100	2001+	QFP100	2315
XC3030APG84BKJ	2001+	PGA	2315
XC3030APC84C-6	2001+	PLCC	2315
XC3030A-PC84C	2001+	PLCC	2315
XC3030APC84C	2001+	PLCC	2315
XC3030APC84BKJ-7I	2001+	PLCC	2315
XC3030APC84BKJ	2001+	PLCC	2315
XC3030APC84BKI	2001+	PLCC	2315
XC3030A-PC84-6C	2001+	PLCC	2315
XC3030APC84-6	2001+	PLCC	2315
XC3030A-PC84	2001+	PLCC	2315
XC3030APC84	2001+	NA	2315
XC3030APC-7 PC44	2001+	PLCC-44L	2315
XC3030APC68BKJ-7I	2001+	PLCC	2315
XC3030APC68BKJ	2001+	BGA	2315
XC3030APC68-7C	2001+	BGA	2315
XC3030APC68-6C	2001+	MODUL	2315
XC3030APC68-3C	2001+	BGA	2315
XC3030A-PC68	2001+	PLCC	2315
XC3030APC68	2001+	BGA	2315
XC3030A-PC44BKJ-6C	2001+	PLCC	2315
XC3030A-PC44BKJ	2001+	PLCC44	2315
XC3030APC44BKI9625	2001+	PLCC44	2315
XC3030A-PC44BBKJ-7I	2001+	PLCC	2315
XC3030A-PC44B	2001+	BGA	2315
XC3030APC44	2001+	PLCC	2315

XC3030A-7PQ44I	2001+	BGA	2315
XC3030A-7PQ100I	2001+	QFP100	2315
XC3030A-7PQ100C	2001+	PQFP100	2315
XC3030A-7PQ-100C	2001+	QFP	2315
XC3030A-7PQ100C	2001+	QFP	2315
XC3030A-7PQ100	2001+	QFP100	2315
XC3030A-7POG100I	2001+	BGA	2315
XC3030A-7PG84M	2001+	PGA	2315
XC3030A-7PG84I	2001+	PGA	2315
XC3030A-7PG84C	2001+	BGA	2315
XC3030A-7PG84B	2001+	PGA	2315
XC3030A-7PCG84I	2001+	PLCC84	2315
XC3030A-7PCG84C	2001+	PLCC84	2315
XC3030A-7PCG68I	2001+	PLCC-68	2315
XC3030A-7PCG68C	2001+	PLCC-68	2315
XC3030A-7PC84I	2001+	PLCC84	2315
XC3030A-7PC84I	2001+	PLCC84	2315
XC3030A-7PC84C	2001+	PLCC84	2315
XC3030A-7PC84C	2001+	PLCC84	2315
XC3030A7PC84C	2001+	BGA	2315
XC3030A-7PC84	2001+	PLCC	2315
XC3030A-7PC68I	2001+	BGA	2315
XC3030A-7PC68C	2001+	PLCC	2315
XC3030A7PC68C	2001+	PLCC	2315
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XC3030A-7PC68	2001+	PLCC	2315
XC3030A7PC68	2001+	PLCC68	2315
XC3030A-7PC44I	2001+	PLCC44	2315
XC3030A-7PC44C	2001+	BGA	2315
XC3030A-7PC44BKJ	2001+	PLCC-44	2315
XC3030A-7PC44	2001+	PLCC	2315
XC3030A-7PC084C	2001+	PLCC	2315
XC3030A-7IVQ64	2001+	QFP	2315
XC3030A-7I/PC68	2001+	PLCC	2315
XC3030A-7CPC84C	2001+	PLCC	2315
XC3030A-7C/PC68	2001+	PLCC	2315
XC3030A-7C	2001+	PLCC	2315
XC3030A-70PLCC68	2001+	PLCC68	2315
XC3030A-70PG84BKJ	2001+	PGA	2315
XC3030A-70PC84C	2001+	PLCC	2315
XC3030A-70PC84	2001+	PLCC	2315