Dynamic Reconfiguration Port (DRP)

Dynamic Reconfiguration of Functional Blocks

Background

In the Virtex-5 family of FPGAs, the configuration memory is used primarily to implement user logic, connectivity, and I/Os, but it is also used for other purposes. For example, it is used to specify a variety of static conditions in functional blocks, such as clock management tiles (CMTs).

Sometimes an application requires a change in these conditions in the functional blocks while the block is operational. This can be accomplished by partial dynamic reconfiguration using the JTAG, ICAP, or SelectMAP ports. However, the dynamic reconfiguration port that is an integral part of each functional block simplifies this process greatly. Such configuration ports exist in the CMTs.

Overview

This document describes the addressable, parallel write/read configuration memory that is implemented in each functional block that might require reconfiguration. This memory has the following attributes:

- It is directly accessible from the FPGA fabric. Configuration bits can be written to and/or read from depending on their function.

- Each bit of memory is initialized with the value of the corresponding configuration memory bit in the bitstream. Memory bits can also be changed later through the ICAP.

- The output of each memory bit drives the functional block logic, so the content of this memory determines the configuration of the functional block.

The address space can include status (read-only) and function enables (write-only). Read-only and write-only operations can share the same address space. Figure 5-1 shows how the configuration bits drive the logic in functional blocks directly in earlier FPGA families, and Figure 5-2 shows how the reconfiguration logic changes the flow to read or write the configuration bits.

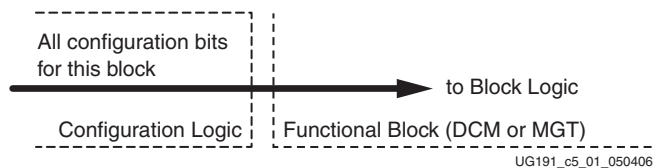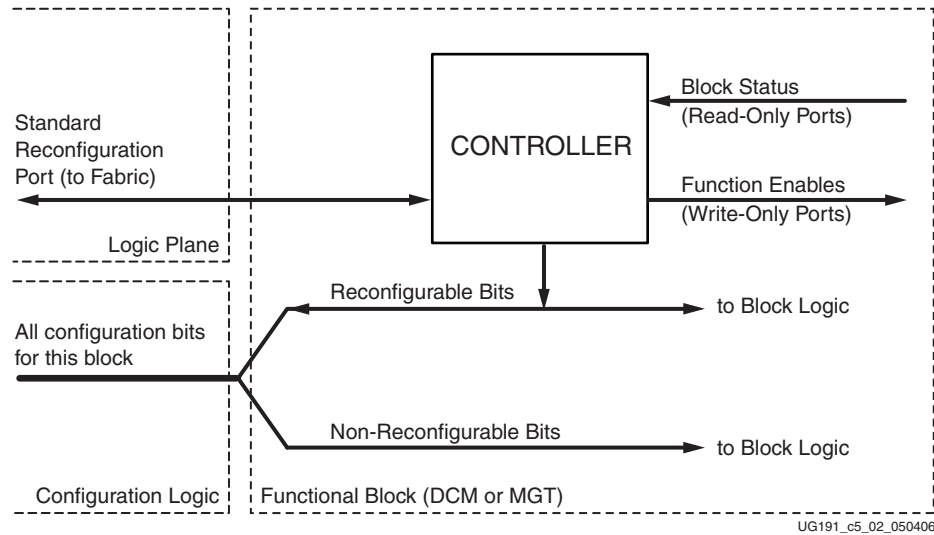*Figure 5-1:* **Block Configuration Logic without Dynamic Interface**

Figure 5-2: **Block Configuration Logic with Dynamic Interface**

Figure 5-3 is the same as Figure 5-2, except the port between the Logic Plane and Functional Block is expanded to show the actual signal names and directions.
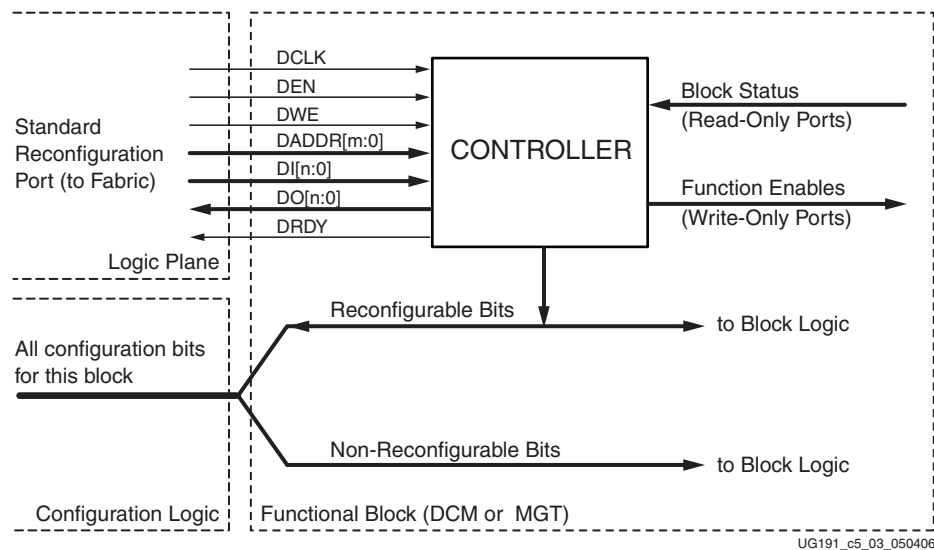

Figure 5-3: **Block Configuration Logic Expanded to Show Signal Names**

FPGA Fabric Port Definition

Table 5-1, page 108, lists each signal on the FPGA Fabric port. The individual functional blocks can implement all or only a subset of these signals. The DCM chapter in the *Virtex-5 User Guide* shows the signals and functions implemented for the specific blocks. In general, the port is a synchronous parallel memory port, with separate read and write buses similar to the block RAM interface. Bus bits are numbered least-significant to most-significant, starting at 0. All signals are active High.

Synchronous timing for the port is provided by the DCLK input, and all the other input signals are registered in the functional block on the rising edge of DCLK. Input (write) data

芯片详细信息

Manufacturer Part Number: XC2VP4-5FF672I	Pbfree Code: 🚫 No	Rohs Code: 🚫 No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA672,26X26,40	Pin Count: 672
Reach Compliance Code: not_compliant	ECCN Code: 3A991.D	HTS Code: 8542.39.00.01	Factory Lead Time: 12 Weeks
Manufacturer: Xilinx	Risk Rank: 5.81	Clock Frequency-Max: 1050 MHz	Combinatorial Delay of a CLB-Max: 0.36 ns
JESD-30 Code: S-PBGA-B672	JESD-609 Code: e0	Length: 27 mm	Moisture Sensitivity Level: 4
Number of CLBs: 752	Number of Inputs: 348	Number of Logic Cells: 6768	Number of Outputs: 348
Number of Terminals: 672	Organization: 752 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA672,26X26,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 225
Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.65 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V
Surface Mount: YES	Technology: CMOS	Terminal Finish: Tin/Lead (Sn63Pb37)	Terminal Form: BALL
Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 27 mm

Table 6-9: **Status Register Description**

Name	Bit Index	Description
BUS_WIDTH	[26:25]	CFG bus width auto detection result. If ICAP is enabled, this field reflects the ICAP bus width after configuration is done. `00` = x1 `01` = x8 `10` = x16 `11` = x32
FS	[24:22]	SPI Flash type select
STARTUP_STATE	[20:18]	CFG startup state machine (0 to 7). Phase 0 = 000 Phase 1 = 001 Phase 2 = 011 Phase 3 = 010 Phase 4 = 110 Phase 5 = 111 Phase 6 = 101 Phase 7 = 100
DEC_ERROR	16	FDRI write attempted before or after decrypt operation: `0:` No DEC_ERROR `1:` DEC_ERROR
ID_ERROR	15	Attempt to write to FDRI without successful DEVICE_ID check. `0:` No ID_ERROR `1:` ID_ERROR
DONE	14	Value on DONE pin
RELEASE_DONE	13	Value of internal DONE signal: `0:` DONE signal not released (pin is actively held Low) `1:` DONE signal released (can be held Low externally)
INIT_B	12	Value on INIT_B pin
INIT_COMPLETE	11	Internal signal indicating initialization has completed: `0:` Initialization has not finished `1:` Initialization finished
MODE	[10:8]	Status of the Mode pins (M[2:0]).
GHIGH_B	7	Status of GHIGH_B: `0:` GHIGH_B asserted `1:` GHIGH_B deasserted
GWE	6	Status of GWE: `0:` FFs and block RAM are write disabled `1:` FFs and block RAM are write enabled

XC3030-7PQ100C	2001+	QFP	2315
XC3030-7PC84I	2001+	PLCC84	2315
XC3030-7PC84C	2001+	QFP	2315
XC3030-7PC68I	2001+	PLCC	2315
XC3030-7PC68C	2001+	PLCC-68	2315
XC3030-7PC44C	2001+	BGA	2315
XC3030-70TQ100I	2001+	QFP	2315
XC3030-70TQ100C	2001+	QFP	2315
XC3030-70PQG100I	2001+	QFP	2315
XC3030-70PQG100C	2001+	QFP	2315
XC3030-70PQ100I	2001+	PQFP100	2315
XC3030-70PQ100C	2001+	PQFP100	2315
XC3030-70PQ100C	2001+	QFP	2315
XC3030-70PG84I	2001+	PGA	2315
XC3030-70PG84C	2001+	PGA	2315
XC3030-70PCG44C	2001+	PLCC-44	2315
XC3030-70PC84I	2001+	PLCC-84	2315
XC3030-70PC84CXCD	2001+	BGA	2315
XC3030-70PC84C	2001+	PLCC68	2315
XC3030-70-PC84C	2001+	PLCC	2315
XC3030-70PC84C	2001+	BGA	2315
XC3030-70PC84 C	2001+	BGA	2315
XC3030-70PC84	2001+	plcc	2315
XC3030-70PC68I	2001+	PLCC68	2315
XC303070PC68C-0213	2001+	BGA	2315
XC3030-70PC68C-0041	2001+	MODUL	2315
XC3030-70PC68C	2001+	PLCC	2315
XC303070PC68C	2001+	BGA	2315
XC3030-70PC68	2001+	PLCC	2315
XC3030-70PC6	2001+	BGA	2315
XC3030-70PC44I	2001+	PLCC44	2315
XC3030-70PC44C G	2001+	DIP	2315
XC3030-70PC44C	2001+	PLCC	2315
XC303070PC44C	2001+	BGA	2315
XC3030-70PC44	2001+	PLCC	2315
XC3030-70PC	2001+	PLCC	2315
XC3030-70C	2001+	PLCC84	2315
XC3030-70/PQ100C	2001+	QFP	2315
XC3030-70 PC84I	2001+	TOS-84	2315
XC3030-70 PC84	2001+	PLCC	2315
XC3030-70	2001+	PLCC	2315