Startup (Step 8)

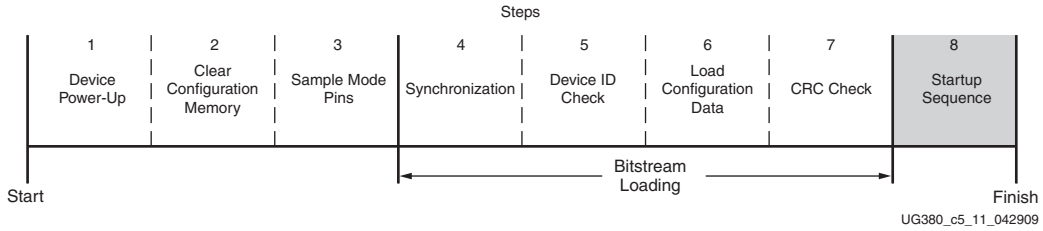

Figure 5-11: **Startup Sequence (Step 8)**

After the configuration frames are loaded, the bitstream asserts the DESYNC command, and then the START command instructs the device to enter the startup sequence. The startup sequence is controlled by an eight-phase (phases 0–7) sequential state machine that is clocked by the JTAG clock or any user clock defined by the BitGen **`-g StartupCLK`** option. The startup sequencer performs the tasks outlined in Table 5-15.

Table 5-15: **User-Selectable Cycle of Startup Events**

Phase	Event
1–6	Wait for DCMs and PLLs to lock (optional)
1–6	Assert Global Write Enable (GWE), allowing RAMs and flip-flops to change state
1–6	Negate Global 3-State (GTS), activating I/O
1–6	Release DONE pin
7	Assert End Of Startup (EOS)

The specific order of startup events (except for EOS assertion) is user-programmable through BitGen options (refer to UG628, *Command Line Tools User Guide*). Table 5-15 shows the general sequence of events, although the specific phase for each of these startup events is user-programmable (EOS is always asserted in the last phase). Refer to Chapter 2, Configuration Interface Basics, for important startup option guidelines. By default, startup events occur as shown in Table 5-16.

Table 5-16: **Default BitGen Sequence of Startup Events**

Phase	Event
4	Release DONE pin
5	Negate GTS, activating I/O
6	Assert GWE, allowing RAMs and flip-flops to change state
7	Assert EOS

The startup sequence can be forced to wait for the DCMs and PLLs to lock with the appropriate BitGen options. These options are typically set to prevent DONE and GWE from being asserted (preventing device operation) before the DCMs and PLLs have locked.

Startup can wait for DCMs and PLLs by assigning the LCK_CYCLE option to a startup phase. If this is not done, startup does not wait for any DCMs or PLLs. When the LCK_CYCLE is set to a startup phase, the FPGA waits for *all* DCMs and PLLs to lock prior to moving to the next phase of startup. To only wait for specific DCMs to lock, assign the STARTUP_WAIT attribute to those instances. There is no corresponding attribute for PLLs. When waiting for DCM and PLL lock, the GTS startup setting must be enabled on a phase before LCK_CYCLE. Failing to do so results in the FPGA waiting for the clock components

Configuration Registers

Table 5-30 summarizes the configuration registers. A detailed explanation of selected registers follows.

Table 5-30: **Configuration Registers**

Register Name	R/W	Address	Description
CRC	W	6'h00	Cyclic Redundancy Check.
FAR_MAJ	W	6'h01	Frame Address Register Block and Major.
FAR_MIN	W	6'h02	Frame Address Register Minor.
FDRI	W	6'h03	Frame Data Input.
FDRO	R	6'h04	Frame Data Output.
CMD	R/W	6'h05	Command.
CTL	R/W	6'h06	Control.
MASK	R/W	6'h07	Control Mask.
STAT	R	6'h08	Status.
LOUT	W	6'h09	Legacy output for serial daisy-chain.
COR1	R/W	6'h0a	Configuration Option 1.
COR2	R/W	6'h0b	Configuration Option 2.
PWRDN_REG	R/W	6'h0c	Power-down Option register.
FLR	W	6'h0d	Frame Length register.
IDCODE	R/W	6'h0e	Product IDCODE.
CWDT	R/W	6'h0f	Configuration Watchdog Timer.
HC_OPT_REG	R/W	6'h10	House Clean Option register.
CSBO	W	6'h12	CSB output for parallel daisy-chaining.
GENERAL1	R/W	6'h13	Power-up self test or loadable program address.
GENERAL2	R/W	6'h14	Power-up self test or loadable program address and new SPI opcode.
GENERAL3	R/W	6'h15	Golden bitstream address.
GENERAL4	R/W	6'h16	Golden bitstream address and new SPI opcode.
GENERAL5	R/W	6'h17	User-defined register for fail-safe scheme.
MODE_REG	R/W	6'h18	Reboot mode.
PU_GWE	W	6'h19	GWE cycle during wake-up from suspend.
PU_GTS	W	6'h1a	GTS cycle during wake-up from suspend.
MFWR	W	6'h1b	Multi-frame write register.
CCLK_FREQ	W	6'h1c	CCLK frequency select for master mode.

Table 5-30: **Configuration Registers *(Cont'd)***

Register Name	R/W	Address	Description
SEU_OPT	R/W	6'h1d	SEU frequency, enable and status.
EXP_SIGN	R/W	6'h1e	Expected readback signature for SEU detection.
RDBK_SIGN	W	6'h1f	Readback signature for readback command and SEU.
BOOTSTS	R	6'h20	Boot History Register.
EYE_MASK	R/W	6'h21	Mask pins for Multi-Pin Wake-Up.
CBC_REG	W	6'h22	Initial CBC Value Register.

CRC Register

The Cyclic Redundancy Check register utilizes a standard 32-bit CRC checksum algorithm to verify bitstream integrity during configuration. If the value written matches the current calculated CRC, the CRC_ERROR flag is cleared and startup is allowed.

FAR_MAJ Register

Frame Address Register sets the starting block and column address for the next configuration data input. See Table 5-31.

Table 5-31: **Frame Address Register (MAJOR)**

	BLK	ROW	MAJOR
Bits	[15:12]	[11:8]	[7:0]
	0xxx	xxxx	xxxxxxxx

FAR_MIN Register

Table 5-32: **Frame Address Register (MINOR)**

	Block RAM	(Reserved)	MINOR
Bits	[15:14]	[13:10]	[9:0]
	xx	0000	xxxxxxxxxx

There are three types of write to FAR:

- Write one word to FAR_MAJ: only updates the FAR_MAJ.
- Write one word to FAR_MIN: only updates the FAR_MIN.
- Write two words to FAR_MAJ: updates both FAR_MAJ and FAR_MIN; the data for FAR_MAJ will come first.

FDRI Register

Configuration data is written to the device by loading the command register with the WCFG command and then loading the Frame Data Input Register.

XC3030-50PQ100C	2001+	QFP-100	2315
XC3030-50PG84M	2001+	PGA	2315
XC3030-50PG84I	2001+	PGA	2315
XC3030-50PC84I	2001+	PLCC84	2315
XC3030-50-PC84C	2001+	BGA	2315
XC3030-50PC84C	2001+	BGA	2315
XC3030-50PC84	2001+	PLCC	2315
XC3030-50PC68I	2001+	PLCC	2315
XC3030-50PC68C	2001+	PLCC68	2315
XC3030-50PC68C	2001+	MODUL	2315
XC3030-50PC44I	2001+	PLCC	2315
XC3030-50PC44C	2001+	PLCC	2315
XC3030-50	2001+	PLCC	2315
XC3030-4VQ100C	2001+	QFP	2315
XC3030-12PC84C	2001+	BGA	2315
XC3030-125TQ100C	2001+	QFP	2315
XC3030-125PQ100C	2001+	QFP	2315
XC3030-125PG84C	2001+	PGA	2315
XC3030-125PC84C	2001+	QFP	2315
XC3030-125PC68C	2001+	BGA	2315
XC3030-125PC100C	2001+	BGA	2315
XC3030-10PQ100C	2001+	QFP100	2315
XC3030-100TQ100I	2001+	QFP	2315
XC3030-100TQ100	2001+	QFP	2315
XC3030-100PQ100Q	2001+	QFP	2315
XC3030-100PQ100I	2001+	QFP	2315
XC3030-100PQ-100C	2001+	QFP	2315
XC3030-100PQ100C	2001+	QFP	2315
XC3030-100PG84M	2001+	PGA	2315
XC3030-100PG84I	2001+	PGA	2315
XC3030-100PG84C	2001+	PGA	2315
XC3030-100PCG44C	2001+	PLCC-44	2315
XC3030-100PC84C	2001+	PLCC	2315
XC3030100PC84C	2001+	BGA	2315
XC3030-100PC84	2001+	PLCC84	2315
XC3030-100PC68I	2001+	MODUL	2315
XC3030-100PC68C	2001+	PLCC68	2315
XC3030-100PC68	2001+	PLCC	2315
XC3030-100PC44I	2001+	PLCC44	2315
XC3030-100PC44C	2001+	PLCC	2315
XC3030-100PC44	2001+	PLCC	2315

XC3020tm-70PQ100C	2001+	QFP	2315
XC3020TM-70PLC68C	2001+	PLCC68	2315
XC3020TM-70PC84	2001+	PLCC	2315
XC3020TM-70PC68I	2001+	PLCC	2315
XC3020TM-70-PC68C	2001+	PLCC	2315
XC3020TM-70PC68BKI	2001+	PLCC	2315
XC3020TM-70PC68	2001+	PLCC	2315
XC3020TM-70C	2001+	PLCC	2315
XC3020TM-70	2001+	BGA	2315
XC3020TM-7	2001+	PLCC	2315
XC3020TM-50PC68I	2001+	PLCC	2315
XC3020TM-50PC68C	2001+	PLCC68	2315
XC3020TM-50	2001+	PLCC	2315
XC3020TM-33PC68I	2001+	PLCC	2315
XC3020TM-125	2001+	PLCC	2315
XC3020TM-10PC68C	2001+	PLCC	2315
XC3020TM-100PC84C	2001+	PLCC	2315
XC3020TM-100PC84	2001+	PLCC	2315
XC3020TM-100PC68I	2001+	DIP68	2315
XC3020TM-100-PC68C	2001+	PLCC	2315
XC3020TM-100PC68C	2001+	PLCC	2315
XC3020TM-100PC68	2001+	PLCC	2315
XC3020TM-100C	2001+	PLCC	2315
XC3020TM-100	2001+	PLCC	2315
XC3020TM	2001+	PLCC	2315
XC3020PQ100BK-100C	2001+	QFP	2315
XC3020PG84C	2001+	PGA	2315
XC3020PC84C	2001+	PLCC	2315
XC3020-PC84BKJ	2001+	BGA	2315
XC3020-PC84BKI	2001+	BGA	2315
XC3020PC84-70C	2001+	BGA	2315
XC3020PC84-50C	2001+	PLCC84	2315
XC3020PC84-100C	2001+	PLCC84	2315
XC3020PC84100C	2001+	BGA	2315
XC3020PC84	2001+	PLCC	2315
XC3020PC68C-70	2001+	PLCC	2315
XC3020PC68-70	2001+	PLCC84	2315
XC3020-PC68	2001+	PLCC	2315
XC3020PC68	2001+	PLCC	2315
XC3020L-8PC84I	2001+	BGA	2315
XC3020L-8PC84C	2001+	PLCC	2315