Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 58 and Table 59) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 60 through Table 63) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 58 and Table 59.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 58: **Recommended Operating Conditions for the DLL**

Symbol		Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18(2)	167(3)	18(2)	167(3)	MHz
	CLKIN_FREQ_DLL_HF		High	48	280(3)	48	280(3)(4)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 100$ MHz	40%	60%	40%	60%	-
			$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation(5)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			High	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL_LF		Period jitter at the CLKIN input	All	–	±1	–	±1	ns
CLKIN_PER_JITT_DLL_HF				–		–		
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See Table 60.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 64.
5. CLKIN input jitter beyond these limits may cause the DCM to lose lock. See UG331 for more details.

Table 59: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All	18	167	18	167	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High		48	280	48	280	MHz
CLKOUT_FREQ_2X_LF(3)	Frequency for the CLK2X and CLK2X180 outputs	Low		36	334	36	334	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low		1.125	110	1.125	110	MHz
CLKOUT_FREQ_DV_HF		High		3	185	3	185	MHz
Output Clock Jitter(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±200	–	±200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±300	–	±300	ps
Duty Cycle								
CLKOUT_DUTY_CYCLE_DLL(5)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	XC3S50	–	±150	–	±150	ps
			XC3S200	–	±150	–	±150	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	–	±150	–	±150	ps
CLKOUT_PHASE	Phase offset between any two DLL outputs (except CLK2X and CLK0)			–	±140	–	±140	ps
	Phase offset between the CLK2X and CLK0 outputs			–	±250	–	±250	ps

XC3020-50CB100B	2001+	PGA	2315
XC3020-50-70	2001+	PLCC	2315
XC3020-50 PC84C	2001+	BGA	2315
XC3020-50 PC68C	2001+	PLCC	2315
XC3020-50	2001+	PQFP100	2315
XC3020-4PC68C	2001+	BGA	2315
XC3020-33PC84C	2001+	PLCC	2315
XC3020-2PQ100C	2001+	QFP	2315
XC3020-125PQ100I	2001+	QFP100	2315
XC3020-125PG84C	2001+	PGA	2315
XC3020-125PG84B	2001+	PGA	2315
XC3020-125PC84C	2001+	BGA	2315
XC3020-125PC68I	2001+	PLCC68	2315
XC3020-125PC68C	2001+	PLCC68	2315
XC3020-100PQG100C	2001+	QFP	2315
XC3020-100PQ100I	2001+	QFP100	2315
XC3020100PQ100I	2001+	QFP100	2315
XC3020-100PG84M	2001+	PGA	2315
XC3020-100PG84I	2001+	PGA	2315
XC3020-100PG84C	2001+	PGA	2315
XC3020-100PG84B	2001+	PGA	2315
XC3020-100PCG84C	2001+	PLCC	2315
XC3020-100PC84I	2001+	PLCC	2315
XC3020-100PC84C	2001+	PLCC	2315
XC3020100PC84C	2001+	PLCC84	2315
XC3020-100PC84	2001+	PLCC	2315
XC3020-100PC68I	2001+	PLCC	2315
XC3020-100PC68C	2001+	PLCC	2315
XC3020100PC68C	2001+	BGA	2315
XC3020-100PC68	2001+	PLCC	2315
XC3020-100PC60C	2001+	QFP	2315
XC3020-100CQ100B	2001+	PGA	2315
XC3020-100CB100M	2001+	原厂原封	2315
XC3020-100CB100B	2001+	NA	2315
XC3020-100	2001+	PLCC	2315
XC3020 TM-70	2001+	PLCC	2315
XC3020 PC68	2001+	PLCC	2315
XC3020 100PC84C	2001+	BGA	2315
XC3020	2001+	PLCC	2315
XC3013A-3PC84C	2001+	PLCC	2315
XC300EFG456	2001+	BGA	2315

XC3020-100CB100B	2001+	NA	2315
XC3020-100	2001+	PLCC	2315
XC3020 TM-70	2001+	PLCC	2315
XC3020 PC68	2001+	PLCC	2315
XC3020 100PC84C	2001+	BGA	2315
XC3020	2001+	PLCC	2315
XC3013A-3PC84C	2001+	PLCC	2315
XC300EFG456	2001+	BGA	2315
XC300EBG432	2001+	BGA	2315
XC300E-6FG456I	2001+	BGA	2315
XC300E-4FG456	2001+	QFP	2315
XC300-6BG352C	2001+	BGA	2315
XC3000L	2001+	BGA	2315
XC3000FM	2001+	BGA	2315
XC3000A/L	2001+	BGA	2315
XC3000A	2001+	BGA	2315
XC3000	2001+	BGA	2315
XC2X150-6FG456C	2001+	BGA-456D	2315
XC2VPX70FF1704	2001+	BGA	2315
XC2VPX70-7FFG1704C	2001+	BGA	2315
XC2VPX70-7FF1704C	2001+	BGA	2315
XC2VPX70-6FFG1704I	2001+	BGA	2315
XC2VPX70-6FFG1704C	2001+	BGA	2315
XC2VPX70-6FF1704I	2001+	BGA	2315
XC2VPX70-6FF1704C	2001+	BGA	2315
XC2VPX70-6FF1704	2001+	BGA	2315
XC2VPX70-5FFG1704I	2001+	BGA	2315
XC2VPX70-5FFG1704C	2001+	BGA	2315
XC2VPX70-5FF1704I	2001+	BGA	2315
XC2VPX70-5FF1704C	2001+	BGA	2315
XC2VPX70	2001+	BGA	2315
XC2VPX20FF896	2001+	BGA	2315
XC2VPX20-7FFG896C	2001+	BGA	2315
XC2VPX20-7FF896C	2001+	BGA	2315
XC2VPX20-6FFG896I	2001+	BGA	2315
XC2VPX20-6FFG896C	2001+	FBGA	2315
XC2VPX20-6FF896I	2001+	BGA	2315
XC2VPX20-6FF896C	2001+	BGA	2315
XC2VPX20-6FF896	2001+	BGA	2315
XC2VPX20-5FFG896I	2001+	BGA	2315
XC2VPX20-5FFG896C	2001+	BGA	2315

Table 72: **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Description</th></tr>
<tr><td>BUSY</td><td>Output</td><td>Configuration Data Rate Control for Parallel Mode:
In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below.
When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state.
<table><tr><th>BUSY</th><th>Function</th></tr><tr><td>0</td><td>The FPGA is ready to accept the next configuration data byte.</td></tr><tr><td>1</td><td>The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte.</td></tr><tr><td>Hi-Z</td><td>If CS_B is High, then BUSY is high impedance.</td></tr></table>This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.</td></tr>
<tr><td>INIT_B</td><td>Bidirectional (open-drain)</td><td>Initializing Configuration Memory/Configuration Error (active-Low):
See description under Serial Configuration Modes, page 112.</td></tr>
</table>

JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.