DDR3 Memory

[Figure 1-2, callout 2]

The memory module at J1 is a 1 GB DDR3 small outline dual-inline memory module (SODIMM). It provides volatile synchronous dynamic random access memory (SDRAM) for storing user code and data.

- Part number: MT8JTF12864HZ-1G6G1 (Micron Technology)
- Supply voltage: 1.5V
- Configuration: 1GB (128 Mb x 64)
- Datapath width: 64 bits
- Data rate: Up to 1,600 MT/s

The VC707 XC7VX485T FPGA memory interface performance is documented in the *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183) [Ref 2].

The DDR3 interface is implemented across I/O banks 37, 38, and 39. Each bank is a 1.5V high-performance bank having a dedicated DCI VRP/N resistor connection. An external 0.75V reference VTTREF is provided for data interface banks 37 and 39. Any interface connected to these banks that requires a reference voltage must use this FPGA voltage reference. The connections between the DDR3 memory and the FPGA are listed in Table 1-4.

Table 1-4: **DDR3 Memory Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
A20	DDR3_A0	SSTL15	98	A0
B19	DDR3_A1	SSTL15	97	A1
C20	DDR3_A2	SSTL15	96	A2
A19	DDR3_A3	SSTL15	95	A3
A17	DDR3_A4	SSTL15	92	A4
A16	DDR3_A5	SSTL15	91	A5
D20	DDR3_A6	SSTL15	90	A6
C18	DDR3_A7	SSTL15	86	A7
D17	DDR3_A8	SSTL15	89	A8
C19	DDR3_A9	SSTL15	85	A9
B21	DDR3_A10	SSTL15	107	A10/AP
B17	DDR3_A11	SSTL15	84	A11
A15	DDR3_A12	SSTL15	83	A12_BC_N
A21	DDR3_A13	SSTL15	119	A13
F17	DDR3_A14	SSTL15	80	A14
E17	DDR3_A15	SSTL15	78	A15
D21	DDR3_BA0	SSTL15	109	BA0
C21	DDR3_BA1	SSTL15	108	BA1

A 2-mm JTAG header (J4) is also provided in parallel for access by Xilinx download cables such as the Platform Cable USB II and the Parallel Cable IV.

The JTAG chain of the VC707 board is illustrated in Figure 1-7. JTAG configuration is allowed at any time regardless of FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin settings at SW11.

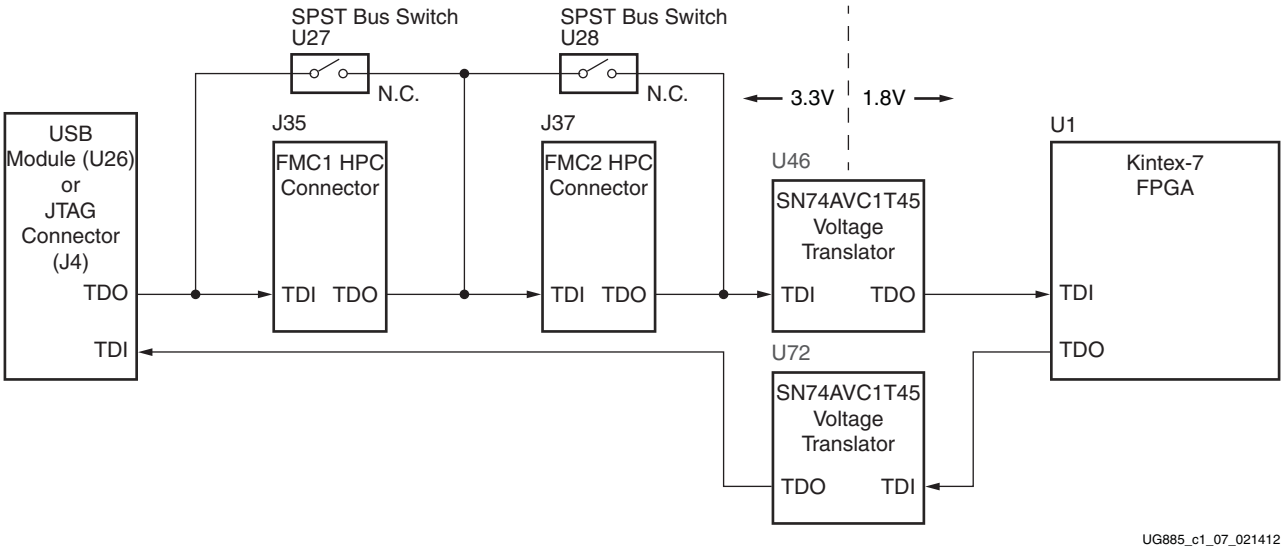

Figure 1-7: **JTAG Chain Block Diagram**

When an FMC mezzanine card is attached to the VC707 board it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U27 and U28. The SPST switches are in a normally closed state and transition to an open state when an FMC mezzanine card is attached. Switch U27 adds an attached FMC1 HPC mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC_PRSNT_M2C_B signal. Switch U28 adds an attached FMC2 HPC mezzanine card to the FPGAs JTAG chain as determined by the FMC2_LPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection via a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.

The JTAG connectivity on the VC707 board allows a host computer to download bitstreams to the FPGA using the Xilinx® iMPACT software. In addition, the JTAG connector allows debug tools such as the Vivado serial I/O analyzer or a software debugger to access the FPGA. The iMPACT software tool can also indirectly program the Linear BPI Flash memory. To accomplish this, the iMPACT software configures the FPGA with a temporary design to access and program the BPI memory device.

The JTAG circuit details are shown in Figure 1-8.

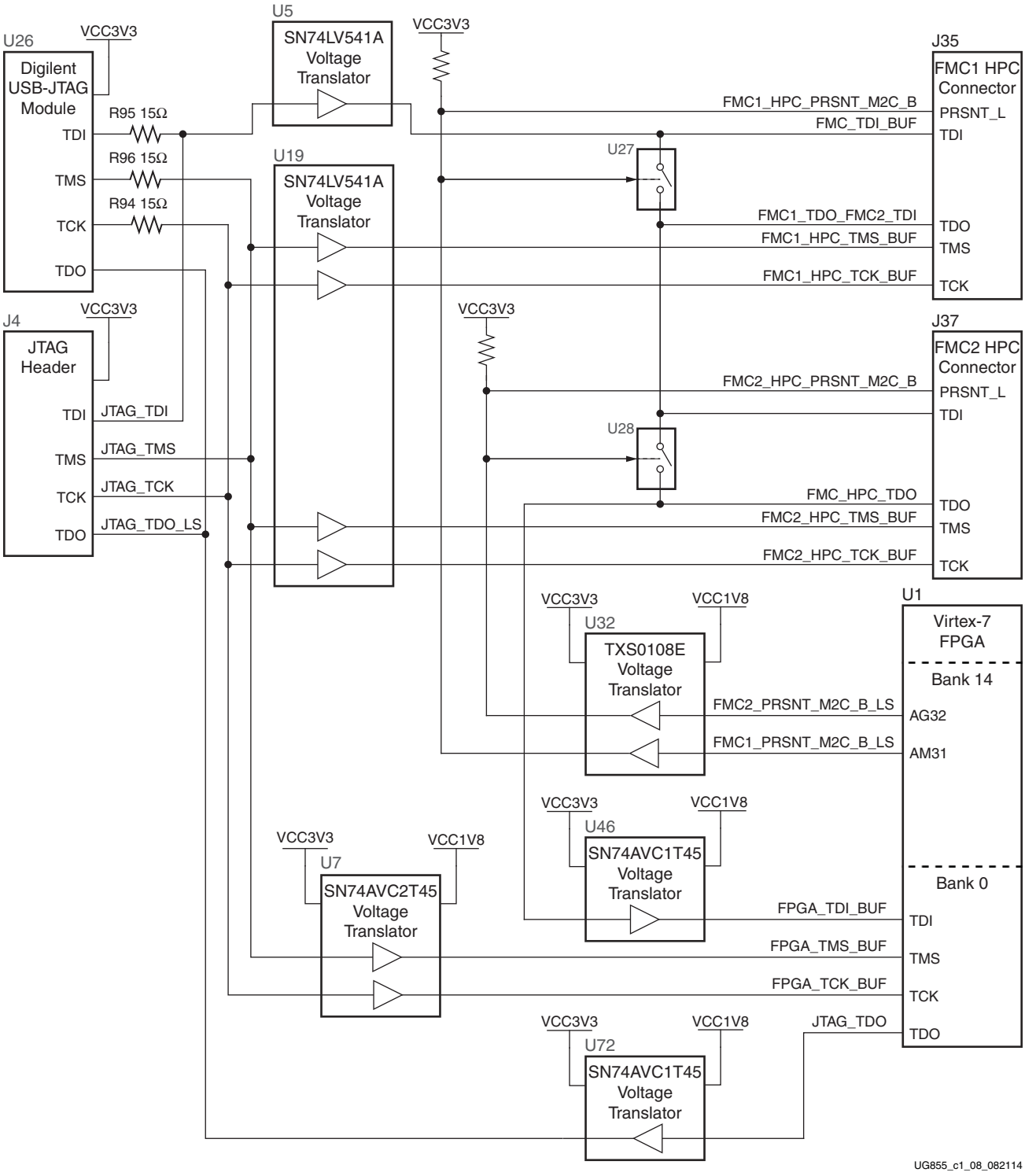

Figure 1-8: **JTAG Circuit**

XC2VPX20-5FFG896I	2001+	BGA	2315
XC2VPX20-5FFG896C	2001+	BGA	2315
XC2VPX20-5FF896I	2001+	BGA	2315
XC2VPX20-5FF896C	2001+	BGA896	2315
XC2VPX20-5FF896	2001+	BGA	2315
XC2VPX20-4FF896I	2001+	BGA	2315
XC2VPX20-4FF896C	2001+	BGA	2315
XC2VPX20-10FF896C	2001+	BGA	2315
XC2VPX20	2001+	BGA	2315
XC2VP80FG256	2001+	BGA	2315
XC2VP80-5FG256I	2001+	BGA	2315
XC2VP7-FGG456	2001+	BGA-316D	2315
XC2VP7FGG456	2001+	BGA	2315
XC2VP7FG668	2001+	BGA	2315
XC2VP7-FG456CGB	2001+	BGA-316D	2315
XC2VP7-FG456A	2001+	BGA	2315
XC2VP7-FG456	2001+	BGA-456D	2315
XC2VP7FG456	2001+	BGA	2315
XC2VP7FFG672	2001+	BGA	2315
XC2VP7FF896CGB	2001+	BGA	2315
XC2VP7-FF896C	2001+	BGA	2315
XC2VP7-FF896	2001+	BGA	2315
XC2VP7FF896	2001+	BGA	2315
XC2VP7-FF672CGB0813	2001+	BGA	2315
XC2VP7FF672CGB	2001+	BGA	2315
XC2VP7FF672	2001+	BGA	2315
XC2VP7-7FGG456I	2001+	BGA456	2315
XC2VP7-7FGG456C	2001+	456-FBGA(23x23)	2315
XC2VP7-7FG456I	2001+	BGA	2315
XC2VP7-7FG456C	2001+	BGA456	2315
XC2VP7-7FFG896I	2001+	BGA896	2315
XC2VP7-7FFG896C	2001+	BGA	2315
XC2VP7-7FFG672I	2001+	BGA	2315
XC2VP7-7FFG672C	2001+	672-FCBGA(27x27)	2315
XC2VP7-7FFG456I	2001+	BGA	2315
XC2VP7-7FF896I	2001+	BGA	2315
XC2VP7-7FF896C	2001+	QFP	2315
XC2VP7-7FF672I	2001+	BGA	2315
XC2VP7-7FF672C	2001+	BGA	2315
XC2VP7-7FF456I	2001+	BGA	2315
XC2VP7-7FF456C	2001+	QFP	2315

XC2VP7-6FG456I	2001+	BGA456	2315
XC2VP7-6FG456C-ES	2001+	BGA	2315
XC2VP7-6-FG456C	2001+	BGA	2315
XC2VP7-6FG456C	2001+	BGA	2315
XC2VP7-6FFG896I	2001+	BGA896	2315
XC2VP7-6FFG896C	2001+	BGA896	2315
XC2VP7-6FFG672I	2001+	BGA	2315
XC2VP7-6FFG672C	2001+	QFP	2315
XC2VP7-6FFG456C	2001+	BGA	2315
XC2VP7-6FF896I	2001+	BGA	2315
XC2VP7-6FF896C	2001+	BGA	2315
XC2VP7-6FF896	2001+	BGA896	2315
XC2VP7-6FF672I	2001+	BGA672	2315
XC2VP7-6FF672C	2001+	BGA	2315
XC2VP7-6FF672	2001+	BGA672	2315
XC2VP7-6FF456I	2001+	BGA	2315
XC2VP7-6FF1517I	2001+	原厂原封	2315
XC2VP7-6FF1517C	2001+	原厂原封	2315
XC2VP7-6F896C	2001+	BGA	2315
XC2VP7-6CFF896	2001+	BGA	2315
XC2VP7-5FGG456I	2001+	BGA	2315
XC2VP7-5FGG456C	2001+	BGA456	2315
XC2VP7-5FG456I	2001+	NA	2315
XC2VP7-5FG456C	2001+	BGA	2315
XC2VP7-5FFG896I	2001+	BGA	2315
XC2VP7-5FFG896C	2001+	TQFP144	2315
XC2VP7-5FFG672I	2001+	BGA	2315
XC2VP7-5FFG672C	2001+	QFP	2315
XC2VP7-5FFG672C	2001+	BGA	2315
XC2VP7-5FF896I	2001+	BGA896	2315
XC2VP7-5FF896C(ES)	2001+	BGA	2315
XC2VP7-5FF896C	2001+	GBA	2315
XC2VP7-5FF896	2001+	BGA	2315
XC2VP7-5FF672I	2001+	BGA	2315
XC2VP7-5FF672C	2001+	BGA	2315
XC2VP7-5FF672	2001+	BGA	2315
XC2VP7-5FF1517C	2001+	BGA	2315
XC2VP7-4FGG456I	2001+	BGA	2315
XC2VP7-4FGG456C	2001+	BGA	2315
XC2VP7-4FG456I	2001+	BGA	2315
XC2VP7-4FG456C	2001+	BGA	2315