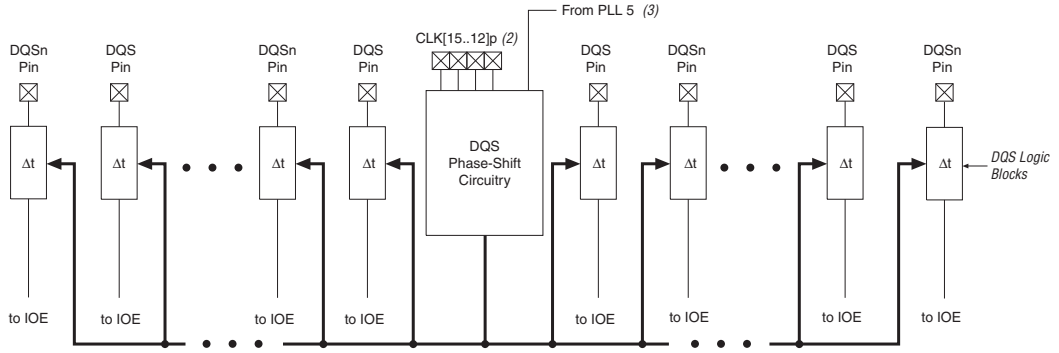
Figure 2–56. DQS Phase-Shift Circuitry *Notes (1), (2), (3), (4)*



Notes to Figure 2–56:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The Δt module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phase-shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–20. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Non-Stratix II	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–20:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–21 through 2–26 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–21 through 2–26 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15

device, PLL 1 can drive a maximum of 10 transmitter channels in I/O bank 1 or a maximum of 19 transmitter channels in I/O banks 1 and 2. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

Table 2–21. EP2S15 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21

Table 2–22. EP2S30 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16
		(3)	29	29	29	29
	Receiver	62 *(2)*	17	14	14	17
		(3)	31	31	31	31

EP4S40G2F40I2N	120	BGA	20+	XILINX
EP4S40G5H40I2N	25	BGA	20+	ALTERA
EP4S40G5H40I2N	40	BGA	20+	Intel/Altera
EP4S40G5H40I2NAD	60	BGA	20+	ALTERA
EP4S40G5H40I4N	220	FBGA1158	20+	ALTERA
EP4SE230F29C4N	8	BGA	20+	ALTERA
EP4SE230F29I3N	60	BGA	20+	ALTERA
EP4SE230F29I4N	68	FCBGA900	20+	ALTERA
EP4SE230F29IN	500	BGA	20+	ALTERA
EP4SE230F35I4N	200	BGA	20+	ALTERA
EP4SE360F35I3N	100	BGA	20+	ALTERA
EP4SE360F35I4N	364	FCBGA1136	20+	ALTERA
EP4SE360F35I4N	1178	LFCSP	20+	ALTERA
EP4SE530H35C4N	22000	SOP8	20+	ALTERA
EP4SE530H35I3N	73	BGA	20+	ALTERA
EP4SE530H35I4N	385	FCBGA1156	20+	ALTERA
EP4SGX110HF35C2N	35	BGA	20+	ALTERA
EP4SGX110HF35C4N	60	BGA	20+	ALTERA
EP4SGX110HF35I3N	50	BGA	20+	ALTERA
EP4SGX180DF29I3N	130	BGA	20+	ALTERA
EP4SGX180DF29I4N	260	FBGA1152	20+	ALTERA
EP4SGX180FF35C3N	176	FCBGA1156	20+	ALTERA
EP4SGX180FF35C4N	156	BGA484	20+	ALTERA
EP4SGX180FF35I3N	21	BGA	20+	ALTERA
EP4SGX180FF35I4N	178	BGA	20+	ALTERA
EP4SGX180KF20C2N	12	BGA	20+	ALTERA
EP4SGX180KF40C2N	5500	1808SMD	20+	ALTERA
EP4SGX180KF40C4N	48	BGA	20+	ALTERA
EP4SGX180KF40I3N	62	BGA	20+	Intel/Altera
EP4SGX180KF40I4N	3197	BGA	20+	ALTERA
EP4SGX230FF35C3N	155	FCBGA1136	20+	ALTERA
EP4SGX230FF35C3N	50	BGA	20+	ALTERA
EP4SGX230FF35C4N	185	BGA	20+	ALTERA
EP4SGX230FF35I3N	120	BGA	20+	ALTERA
EP4SGX230FF35I3N	101	BGA	20+	ALTERA
EP4SGX230FF35I4N	500	BGA	20+	ALTERA
EP4SGX230FF35I4N	100	BGA	20+	ALTERA

EP4SGX230KF40C4N	145	BGA	20+	ALTERA
EP4SGX230KF40C4N	58	BGA	20+	Intel/Altera
EP4SGX230KF40I3N	180	BGA	20+	ALTERA
EP4SGX230KF40I3N	840	BGA	20+	ALTERA
EP4SGX230KF40I4N	277	BGA2397	20+	XILINX
EP4SGX230KF40I4N	231	FCBGA900	20+	ALTERA
EP4SGX290KF40C2N	2000	BGA	20+	ALTERA
EP4SGX290KF40C3N	42000	SOT-353	20+	ALTERA
EP4SGX290NF45I3N	280	BGA	20+	ALTERA
EP4SGX360FF35C3N	1000	BGA	20+	ALTERA
EP4SGX360FF35C4N	25	BGA	20+	ALTERA
EP4SGX360FF35I4N	500	DIP	20+	ALTERA
EP4SGX360FH29C3N	178	BGA	20+	ALTERA
EP4SGX360HF35C2N	200	QFN64	20+	ALTERA
EP4SGX360HF35C3N	50	BGA	20+	ALTERA
EP4SGX360HF35C4N	2000	BGA64	20+	ALTERA
EP4SGX360HF35I3N	184	DIP-4	20+	ALTERA
EP4SGX360HF35I4N	2900	TSSOP24	20+	ALTERA
EP4SGX360KF40C2N	68	BGA	20+	ALTERA
EP4SGX360KF40C3N	72	BGA	20+	ALTERA
EP4SGX360KF40C4N	102	FBGA1152	20+	ALTERA
EP4SGX360KF40I3N	120	FBGA1158	20+	ALTERA
EP4SGX360KF40I4N	2900	QFP64	20+	ALTERA
EP4SGX360KF43I3N	172	FBGA1148	20+	ALTERA
EP4SGX360NF45I3N	341	FCBGA1136	20+	ALTERA
EP4SGX530HH35C2N	276	BGA	20+	ALTERA
EP4SGX530HH35C3N	1	BGA	20+	ALTERA
EP4SGX530HH35C4N	200	BGA	20+	ALTERA
EP4SGX530HH35I3N	172	BGA	20+	ALTERA
EP4SGX530HH35I4N	155	BGA	20+	ALTERA
EP4SGX530KH40C2N	228	BGA	20+	ALTERA
EP4SGX530KH40C3N	145	FCBGA1153	20+	ALTERA
EP4SGX530KH40C3N	50	BGA	20+	ALTERA
EP4SGX530KH40I3N	120	BGA900	20+	XILINX
EP4SGX530KH40I3N	1500	SOP-8	20+	ALTERA
EP4SGX530KH40I4N	120	BGA	20+	ALTERA
EP4SGX530NF45C2N	80	BGA	20+	XILINX