Programmable IOE Delay

Table 1–41 shows Stratix III IOE programmable delay settings. For more information on the annotation of delays in the IOE, refer to Figure 7–7 in the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

Table 1–41. Stratix III IOE Programmable Delay *(Note 1)*

Parameter	Available Settings	Min Offset *(2)*	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Unit
			Industrial	Commercial	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
			Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	Max Offset	
D1	15	0	442	491	748	829	916	871	833	870	957	915	833	ps
D2	7	0	248	285	387	412	442	427	411	433	464	448	411	ps
D3	7	0	1625	1806	2747	3058	3371	3218	3084	3210	3540	3382	3084	ps
D4	15	0	491	517	726	872	884	844	808	845	928	887	808	ps
D5	15	0	452	503	764	801	930	887	850	889	977	932	850	ps
D6	6	0	179	199	305	337	370	354	339	354	389	371	339	ps

Notes to Table 1–41:

(1) You can set the parameter values in the Quartus II software by selecting D1, D2, D3, D4, D5, and D6 in the Assignment Name column.

(2) The minimum offset represented in the table does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 1–42 lists the delay chain settings that control the rising and falling edge delays of the output buffer. Default delay is 0 ps.

Table 1–42. Programmable Output Buffer Delay *(Note 1)*

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or Falling Edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Note to Table 1–42:

(1) You can set the programmable output buffer delay in the Quartus II software by selecting the 'Output Buffer Delay Control' assignment to either positive, negative or both edges with the specific values as stated in the table above in ps for the 'Output Buffer Delay' assignment.

User I/O Pin Timing

Table 1–43 through Table 1–142 show user I/O pin timing for Stratix III devices. I/O buffer t_{su}, t_h, and t_{co} are reported for the cases when I/O clock is driven by a non-PLL global clock (GCLK) and a PLL driven global clock (GCLK-PLL). For t_{su}, t_h and t_{co} using regional clock, add the value from the adder tables listed for each device to the GCLK/GCLK-PLL values for the device.

Table 1–46 specifies EP3SL50 row pins output timing parameters for single-ended I/O standards.

Table 1–46. EP3SL50 Row Pins output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.3-V LVTTL	4mA	GCLK	t_{co}	3.197	3.438	4.781	5.176	5.684	5.549	5.751	5.305	5.818	5.682	5.828	ns
		GCLK PLL	t_{co}	1.482	1.677	2.061	2.175	2.372	2.388	2.308	2.295	2.495	2.512	2.303	ns
	8mA	GCLK	t_{co}	3.104	3.333	4.651	5.038	5.540	5.405	5.607	5.164	5.669	5.533	5.679	ns
		GCLK PLL	t_{co}	1.415	1.606	1.951	2.037	2.228	2.244	2.164	2.154	2.346	2.363	2.154	ns
	12mA	GCLK	t_{co}	3.014	3.233	4.532	4.915	5.412	5.277	5.479	5.037	5.537	5.401	5.547	ns
		GCLK PLL	t_{co}	1.336	1.517	1.845	1.930	2.100	2.116	2.036	2.046	2.214	2.260	2.022	ns
3.3-V LVCMOS	4mA	GCLK	t_{co}	3.207	3.442	4.789	5.181	5.689	5.554	5.756	5.311	5.823	5.687	5.833	ns
		GCLK PLL	t_{co}	1.492	1.684	2.065	2.180	2.377	2.393	2.313	2.301	2.500	2.517	2.308	ns
	8mA	GCLK	t_{co}	3.018	3.237	4.538	4.921	5.418	5.283	5.485	5.043	5.544	5.408	5.554	ns
		GCLK PLL	t_{co}	1.340	1.521	1.856	1.945	2.106	2.122	2.042	2.058	2.221	2.269	2.029	ns
3.0-V LVTTL	4mA	GCLK	t_{co}	3.151	3.384	4.733	5.129	5.641	5.506	5.708	5.262	5.776	5.640	5.786	ns
		GCLK PLL	t_{co}	1.442	1.638	2.028	2.128	2.329	2.345	2.265	2.252	2.453	2.470	2.261	ns
	8mA	GCLK	t_{co}	3.026	3.257	4.580	4.970	5.477	5.342	5.544	5.100	5.612	5.475	5.621	ns
		GCLK PLL	t_{co}	1.341	1.526	1.891	1.969	2.165	2.181	2.101	2.090	2.289	2.305	2.096	ns
	12mA	GCLK	t_{co}	2.987	3.206	4.498	4.887	5.389	5.254	5.456	5.014	5.519	5.382	5.528	ns
		GCLK PLL	t_{co}	1.304	1.488	1.831	1.903	2.077	2.093	2.013	2.016	2.196	2.222	2.003	ns
3.0-V LVCMOS	4mA	GCLK	t_{co}	3.065	3.303	4.627	5.022	5.530	5.395	5.597	5.154	5.665	5.528	5.674	ns
		GCLK PLL	t_{co}	1.363	1.550	1.926	2.021	2.218	2.234	2.154	2.144	2.342	2.358	2.149	ns
	8mA	GCLK	t_{co}	2.969	3.188	4.463	4.848	5.350	5.215	5.417	4.974	5.479	5.342	5.488	ns
		GCLK PLL	t_{co}	1.291	1.472	1.803	1.874	2.038	2.054	1.974	1.986	2.156	2.193	1.963	ns
2.5 V	4mA	GCLK	t_{co}	3.177	3.420	4.865	5.283	5.813	5.678	5.880	5.422	5.955	5.818	5.964	ns
		GCLK PLL	t_{co}	1.468	1.675	2.136	2.282	2.501	2.517	2.437	2.412	2.632	2.648	2.439	ns
	8mA	GCLK	t_{co}	3.067	3.321	4.710	5.120	5.643	5.508	5.710	5.255	5.781	5.644	5.790	ns
		GCLK PLL	t_{co}	1.383	1.572	2.012	2.119	2.331	2.347	2.267	2.245	2.458	2.474	2.265	ns
	12mA	GCLK	t_{co}	3.021	3.245	4.599	5.001	5.517	5.382	5.584	5.132	5.651	5.514	5.660	ns
		GCLK PLL	t_{co}	1.326	1.528	1.928	2.015	2.205	2.221	2.141	2.132	2.328	2.354	2.135	ns

Table 1–50. EP3SL50 Row Pins output Timing Parameters (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RSDS_E_1R	—	GCLK	t_{co}	3.043	3.268	4.622	5.029	5.547	5.404	5.603	5.160	5.681	5.537	5.667	ns
		GCLK PLL	t_{co}	1.386	1.572	1.990	2.086	2.294	2.306	2.216	2.204	2.418	2.426	2.201	ns
RSDS_E_3R	—	GCLK	t_{co}	3.025	3.258	4.660	5.075	5.601	5.458	5.657	5.211	5.742	5.598	5.728	ns
		GCLK PLL	t_{co}	1.368	1.562	2.028	2.132	2.348	2.360	2.270	2.255	2.479	2.487	2.262	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.079	3.311	4.706	5.119	5.644	5.501	5.700	5.254	5.781	5.637	5.767	ns
		GCLK PLL	t_{co}	1.402	1.595	2.054	2.156	2.371	2.383	2.293	2.278	2.498	2.506	2.281	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{co}	3.065	3.297	4.693	5.106	5.631	5.488	5.687	5.240	5.768	5.624	5.754	ns
		GCLK PLL	t_{co}	1.388	1.581	2.041	2.143	2.358	2.370	2.280	2.264	2.485	2.493	2.268	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{co}	3.061	3.293	4.691	5.106	5.632	5.489	5.688	5.240	5.770	5.626	5.756	ns
		GCLK PLL	t_{co}	1.384	1.577	2.039	2.143	2.359	2.371	2.281	2.264	2.487	2.495	2.270	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{co}	3.077	3.308	4.692	5.103	5.626	5.483	5.682	5.237	5.763	5.619	5.749	ns
		GCLK PLL	t_{co}	1.400	1.592	2.040	2.140	2.353	2.365	2.275	2.261	2.480	2.488	2.263	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{co}	3.066	3.298	4.688	5.099	5.623	5.480	5.679	5.234	5.760	5.616	5.746	ns
		GCLK PLL	t_{co}	1.389	1.582	2.036	2.136	2.350	2.362	2.272	2.258	2.477	2.485	2.260	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{co}	3.063	3.295	4.686	5.097	5.621	5.478	5.677	5.232	5.759	5.615	5.745	ns
		GCLK PLL	t_{co}	1.386	1.579	2.034	2.134	2.348	2.360	2.270	2.256	2.476	2.484	2.259	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.074	3.305	4.687	5.098	5.620	5.477	5.676	5.231	5.757	5.613	5.743	ns
		GCLK PLL	t_{co}	1.397	1.589	2.035	2.135	2.347	2.359	2.269	2.255	2.474	2.482	2.257	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{co}	3.064	3.296	4.685	5.096	5.619	5.476	5.675	5.231	5.757	5.613	5.743	ns
		GCLK PLL	t_{co}	1.387	1.580	2.033	2.133	2.346	2.358	2.268	2.255	2.474	2.482	2.257	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{co}	3.050	3.282	4.670	5.081	5.605	5.462	5.661	5.216	5.742	5.598	5.728	ns
		GCLK PLL	t_{co}	1.373	1.566	2.018	2.118	2.332	2.344	2.254	2.240	2.459	2.467	2.242	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{co}	3.047	3.278	4.666	5.077	5.601	5.458	5.657	5.212	5.738	5.594	5.724	ns
		GCLK PLL	t_{co}	1.370	1.562	2.014	2.114	2.328	2.340	2.250	2.236	2.455	2.463	2.238	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{co}	3.044	3.276	4.667	5.080	5.604	5.461	5.660	5.215	5.742	5.598	5.728	ns
		GCLK PLL	t_{co}	1.367	1.560	2.015	2.117	2.331	2.343	2.253	2.239	2.459	2.467	2.242	ns

RoHS:	N	
产品:	Stratix II	☐
系列:	Stratix II EP2S130	☐
逻辑元件数量:	132540 LE	☐
自适应逻辑模块 - ALM:	53016 ALM	☐
嵌入式内存:	6.44 Mbit	☐
输入/输出端数量:	742 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-1020	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	6627 LAB	
工作电源电流:	820 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	24	
子类别:	Programmable Logic ICs	
总内存:	6747840 bit	
商标名:	Stratix II	
零件号别名:	970067	

芯片详细信息

Manufacturer Part Number: EP2S130F1020C4	Rohs Code: No	Part Life Cycle Code: Not Recommended	Ihs Manufacturer: INTEL CORP
Package Description: 33 X 33 MM, 1 MM PITCH, FBGA-1020	Reach Compliance Code: compliant	ECCN Code: 3A001.A.7.A	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 7.83	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 5.117 ns
JESD-30 Code: S-PBGA-B1020	JESD-609 Code: e0	Length: 33 mm	Moisture Sensitivity Level: 3
Number of CLBs: 53016	Number of Inputs: 742	Number of Logic Cells: 132540	Number of Outputs: 734
Number of Terminals: 1020	Operating Temperature-Max: 85 °C	Organization: 53016 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA1020,32X32,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 220	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 3.5 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: TIN LEAD	Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 30	Width: 33 mm		