C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–18 shows the Stratix II GX device's routing scheme.

Table 2–18. Stratix II GX Device Routing Scheme (Part 1 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain										✓						
Carry chain										✓						
Register chain										✓						
Local interconnect										✓	✓	✓	✓	✓	✓	✓
Direct link interconnect				✓												
R4 interconnect				✓		✓	✓	✓	✓							
R24 interconnect						✓	✓	✓	✓							
C4 interconnect				✓		✓		✓								
C16 interconnect						✓	✓	✓	✓							
ALM	✓	✓	✓	✓	✓	✓		✓								
M512 RAM block				✓	✓	✓		✓								
M4K RAM block				✓	✓	✓		✓								
M-RAM block					✓	✓	✓	✓								
DSP blocks					✓	✓		✓								

Table 2–18. Stratix II GX Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–19 shows the size and features of the different RAM blocks.

Table 2–19. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	420 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	

Table 2–20 shows the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

Table 2–20. M-RAM Row Interface Unit Signals

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

Refer to the *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on TriMatrix memory.

芯片详细信息

Manufacturer Part Number: EP2S130F1020C3	Rohs Code: No	Part Life Cycle Code: Not Recommended	Ihs Manufacturer: INTEL CORP
Package Description: 33 X 33 MM, 1 MM PITCH, FBGA-1020	Reach Compliance Code: compliant	ECCN Code: 3A001.A.7.A	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.29	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 4.672 ns
JESD-30 Code: S-PBGA-B1020	JESD-609 Code: e0	Length: 33 mm	Moisture Sensitivity Level: 3
Number of CLBs: 53016	Number of Inputs: 742	Number of Logic Cells: 132540	Number of Outputs: 734
Number of Terminals: 1020	Operating Temperature-Max: 85 °C	Organization: 53016 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA1020,32X32,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 220	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 3.5 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: Tin/Lead (Sn/Pb)	Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 30	Width: 33 mm		

RoHS:	N	
产品:	Stratix II	☐
系列:	Stratix II EP2S130	☐
逻辑元件数量:	132540 LE	☐
自适应逻辑模块 - ALM:	53016 ALM	☐
嵌入式内存:	6.44 Mbit	☐
输入/输出端数量:	742 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-1020	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	6627 LAB	
工作电源电流:	820 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	24	
子类别:	Programmable Logic ICs	
总内存:	6747840 bit	
商标名:	Stratix II	
零件号别名:	966852	