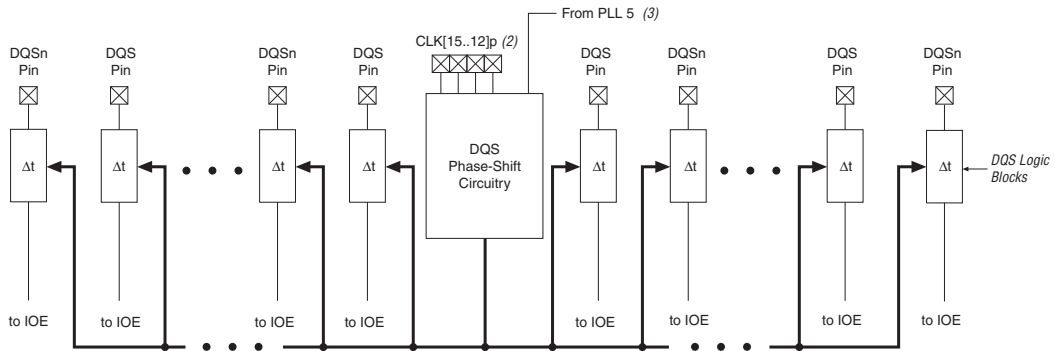*Figure 2–56. DQS Phase-Shift Circuitry*   *Notes (1), (2), (3), (4)*

Notes to *Figure 2–56*:
(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.
(2) The Δt module represents the DQS logic block.
(3) Clock pins CLK[15..12]p feed the phase-shift circuitry on the top of the device and clock pins CLK[7..4]p feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phase-shift circuitry.
(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–20. Supported TDO/TDI Voltage Combinations (Part 2 of 2)						
Device	**TDI Input Buffer Power**	**Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4**				
		V_{CCIO} = 3.3 V	**V_{CCIO} = 2.5 V**	**V_{CCIO} = 1.8 V**	**V_{CCIO} = 1.5 V**	**V_{CCIO} = 1.2 V**
Non-Stratix II	VCC = 3.3 V	✓ *(1)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ *(1), (4)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ *(1), (4)*	✓ *(2), (5)*	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ *(1), (4)*	✓ *(2), (5)*	✓ *(6)*	✓	✓

Notes to Table 2–20:
(1)   The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2)   The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3)   An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4)   Input buffer must be 3.3-V tolerant.
(5)   Input buffer must be 2.5-V tolerant.
(6)   Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–21 through 2–26 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–21 through 2–26 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15

Document Revision History

Table 2–27 shows the revision history for this chapter.

Table 2–27. Document Revision History (Part 1 of 2)		
Date and Document Version	**Changes Made**	**Summary of Changes**
May 2007, v4.3	Updated "Clock Control Block" section.	—
	Updated note in the "Clock Control Block" section.	—
	Deleted Tables 2-11 and 2-12.	—
	Updated notes to: ● Figure 2–41 ● Figure 2–42 ● Figure 2–43 ● Figure 2–45	—
	Updated notes to Table 2–18.	—
	Moved Document Revision History to end of the chapter.	—
August 2006, v4.2	Updated Table 2–18 with note.	—
April 2006, v4.1	● Updated Table 2–13. ● Removed Note 2 from Table 2–16. ● Updated "On-Chip Termination" section and Table 2–19 to include parallel termination with calibration information. ● Added new "On-Chip Parallel Termination with Calibration" section. ● Updated Figure 2–44.	● Added parallel on-chip termination description and specification. ● Changed RCLK names to match the Quartus II software in Table 2–13.
December 2005, v4.0	Updated "Clock Control Block" section.	—
July 2005, v3.1	● Updated HyperTransport technology information in Table 2–18. ● Updated HyperTransport technology information in Figure 2–57. ● Added information on the asynchronous clear signal.	—
May 2005, v3.0	● Updated "Functional Description" section. ● Updated Table 2–3. ● Updated "Clock Control Block" section. ● Updated Tables 2–17 through 2–19. ● Updated Tables 2–20 through 2–22. ● Updated Figure 2–57.	—
March 2005, 2.1	● Updated "Functional Description" section. ● Updated Table 2–3.	—

RoHS:	[RoHS] 详细信息	
产品:	Stratix II	☐
系列:	Stratix II EP2S130	☐
逻辑元件数量:	132540 LE	☐
自适应逻辑模块 - ALM:	53016 ALM	☐
嵌入式内存:	6.44 Mbit	☐
输入/输出端数量:	534 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-780	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	6627 LAB	
工作电源电流:	820 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	36	
子类别:	Programmable Logic ICs	
总内存:	6747840 bit	
商标名:	Stratix II	
零件号别名:	970070	

芯片详细信息

Manufacturer Part Number: EP2S130F780C4N	Pbfree Code: 🟢 Yes	Rohs Code: 🟢 Yes	Part Life Cycle Code: Transferred
Ihs Manufacturer: ALTERA CORP	Part Package Code: BGA	Package Description: 29 X 29 MM, 1 MM PITCH, LEAD FREE, FBGA-780	Pin Count: 780
Reach Compliance Code: compliant	ECCN Code: 3A001.A.7.A	HTS Code: 8542.39.00.01	Manufacturer: Altera Corporation
Risk Rank: 5.25	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 5.117 ns	JESD-30 Code: S-PBGA-B780
JESD-609 Code: e1	Length: 29 mm	Moisture Sensitivity Level: 3	Number of CLBs: 6627
Number of Inputs: 534	Number of Logic Cells: 132540	Number of Outputs: 526	Number of Terminals: 780
Operating Temperature-Max: 85 °C	Organization: 6627 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA780,28X28,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 245
Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.5 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V
Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: TIN SILVER COPPER
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature- Max (s): 40
Width: 29 mm			