Applications and Protocols Supported with Stratix II GX Devices

Each Stratix II GX transceiver block is designed to operate at any serial bit rate from 600 Mbps to 6.375 Gbps per channel. The wide data rate range allows Stratix II GX transceivers to support a wide variety of standards and protocols, such as PCI Express, GIGE, SONET/SDH, SDI, OIF-CEI, and XAUI. Stratix II GX devices are ideal for many high-speed communication applications, such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications links.

Example Applications Support for Stratix II GX

Stratix II GX devices can be used for many applications, including:

- Traffic management with various levels of quality of service (QoS) and integrated serial backplane interconnect
- Multi-port single-protocol switching (for example, PCI Express, GIGE, XAUI switch, or SONET/SDH)

Logic Array Blocks

Each logic array block (LAB) consists of eight adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnects, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in a LAB. The Quartus II Compiler places associated logic in a LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Table 2–17 shows Stratix II GX device resources. Figure 2–32 shows the Stratix II GX LAB structure.

Table 2–17. Stratix II GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2SGX30	6/202	4/144	1	2/16	49	36
EP2SGX60	7/329	5/255	2	3/36	62	51
EP2SGX90	8/488	6/408	4	3/48	71	68
EP2SGX130	9/699	7/609	6	3/63	81	87

EP2AGX65DF29C6N	116	FCBGA1517	20+	ALTERA
EP2AGX65DF29I3N	60	BGA	20+	Intel/Altera
EP2AGX65DF29I3N	133	FCBGA1517	20+	ALTERA
EP2AGX65DF29I5N	172	BGA	20+	ALTERA
EP2AGX95DF25C4N	200	FCBGA	20+	ALTERA
EP2AGX95DF25C6N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I5N	58	FPBGA1020	20+	ALTERA
EP2AGX95EF29C4N	1080	BGA	20+	ALTERA
EP2AGX95EF29C5N	50	BGA	20+	Intel/Altera
EP2AGX95EF29C5N	50	BGA	20+	ALTERA
EP2AGX95EF29C6N	15	BGA	20+	ALTERA
EP2AGX95EF29I3N	72	FBGA1156	20+	ALTERA
EP2AGX95EF35C6N	455	FBGA1152	20+	ALTERA
EP2AGX95EF35I3N	400	DIP	20+	ALTERA
EP2AGX95EF35I5N	426	BGA1152	20+	ALTERA
EP2AGZ300FF35I3N	500	TO220-7	20+	ALTERA
EP2AGZ300FH29I3N	4000	DIP16	20+	ALTERA
EP2AGZ300HF40I3N	1400	SOP	20+	ALTERA
EP2AGZ300HF40I4N	1500	PWRSO-10	20+	ALTERA
EP2AGZ350FF35I3N	50	BGA	20+	ALTERA
EP2AGZ350FF35I4N	14000	TSSOP20	20+	ALTERA
EP2AGZ350FH29I3N	350	SOT233	20+	ALTERA
EP2AGZ350FH29I4N	60000	DIP-8	20+	ALTERA
EP2AGZ350HF40I3N	3000	SMD	20+	ALTERA
EP2AGZ350HF40I4N	5800	SMD	20+	ALTERA
EP2S130F1020C3N	160	FCBGA	20+	ALTERA
EP2S130F1020C4N	200	BGA	20+	ALTERA
EP2S130F1020C5N	237	FCBGA1738	20+	ALTERA
EP2S130F1020I4	300	BGA	20+	ALTERA
EP2S130F1020I4N	34	BGA	20+	ALTERA/INTER
EP2S130F1020I4N	252	BGA	20+	ALTERA
EP2S15F484C4	200	FBGA	20+	ALTERA
EP2S15F484C4N	109	FBGA	20+	ALTERA
EP2S15F484C5	200	BGA	20+	ALTERA
EP2S15F484C5N	120	FCBGA	20+	ALTERA

EP2S60F672I4N	347	FCBGA668	20+	ALTERA
EP2S60F672I5	3000	BGA	20+	ALTERA
EP2S60F672I5N	116	FBGA676	20+	ALTERA
EP2S90F1020C3	122	BGA	20+	ALTERA
EP2S90F1020C3N	120	FBGA	20+	ALTERA
EP2S90F1020C4	120	FBGA	20+	ALTERA
EP2S90F1020C4N	300	FBGA	20+	ALTERA
EP2S90F1020C4N	300	BGA	20+	ALTERA
EP2S90F1020C5N	368	FCBGA1156	20+	ALTERA
EP2S90F1020I3N	482	BGA	20+	ALTERA
EP2S90F1020I4N	897	BGA	20+	ALTERA
EP2S90F1020I4N	50	BGA	20+	ALTERA/INTER
EP2S90F1020I4N	283	FCBGA901	20+	ALTERA
EP2S90F1508C5N	448	BGA	20+	ALTERA
EP2SGX130GF1508C3N	6	BGA	20+	Intel/Altera
EP2SGX130GF1508C3N	109	FCBGA900	20+	ALTERA
EP2SGX130GF1508C4N	80	BGA	20+	ALTERA
EP2SGX130GF1508C5N	488	BGA	20+	ALTERA
EP2SGX130GF1508I4N	47	BGA	20+	Intel/Altera
EP2SGX130GF1508I4N	280	BGA	20+	ALTERA
EP2SGX30DF780I4N	63	FBGA1761	20+	ALTERA
EP2SGX60CF780I4	69	BGA	20+	ALTERA
EP2SGX60EF1152C3N	163	BGA	20+	ALTERA
EP2SGX60EF1152C3N	50	BGA	20+	Intel/Altera
EP2SGX60EF1152C4N	120	BGA	20+	ALTERA
EP2SGX60EF1152C4N	57	BGA	20+	Intel/Altera
EP2SGX60EF1152C5N	200	BGA	20+	ALTERA
EP2SGX60EF1152I3N	120	BGA	20+	ALTERA
EP2SGX60EF1152I4N	347	FCBGA900	20+	ALTERA
EP2SGX90EF1152C3N	186	BGA	20+	ALTERA
EP2SGX90EF1152C3N	33	BGA	20+	Intel/Altera
EP2SGX90EF1152C4N	212	BGA	20+	ALTERA
EP2SGX90EF1152C4N	1000	BGA	20+	ALTERA
EP2SGX90EF1152I4N	16	BGA	20+	Intel/Altera
EP2SGX90EF1152I4N	98	FCBGA1158	20+	ALTERA
EP2SGX90FF1508C3N	10	BGA	20+	ALTERA
EP3SE110F1152C2N	88	BGA	20+	ALTERA

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Stratix II GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Stratix II GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix II GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

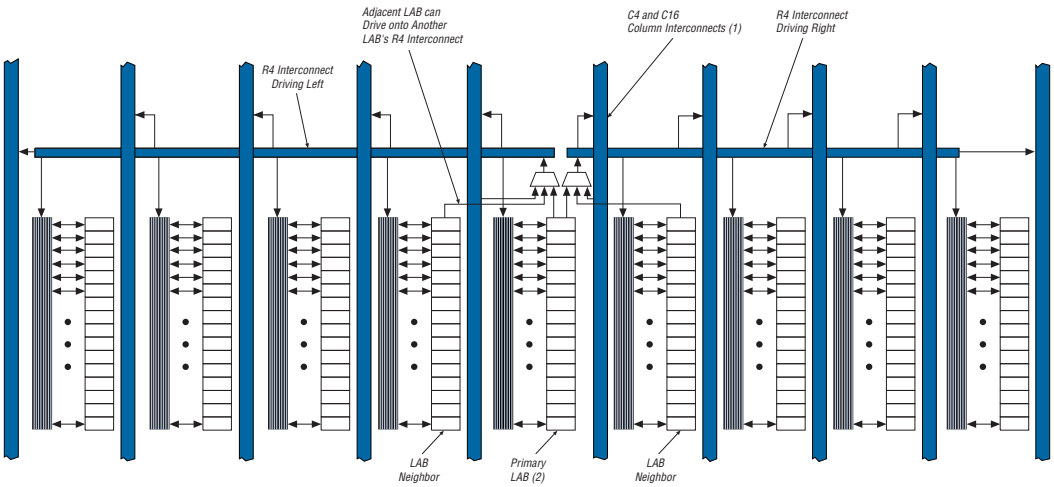
- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–46 shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–46. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 2–46:

(1) C4 and C16 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.
(3) The LABs in Figure 2–46 show the 16 possible logical outputs per LAB.