Table 2. TI-ALS Design Configurations (see Note 1)

HARDWARE PLATFORM	LIBRARY/CAE HOST ENVIRONMENT	DESIGN SUPPORT (gates)		TI SUSTEM PART NUMBER
		UP TO 2500	UP TO 10000	
386/486-based PC	View*Logic*	X		TPC-ALS-DS–PC-VL
	View*Logic*		X	TPC-ALS-DA–PC-VL
	OrCAD	X		TPC-ALS-DS–PC-OR
	OrCAD		X	TPC-ALS-DA–PC-OR
Sun	Cadence		X	TPC-ALS-DA–SN-CD
	Mentor		X	TPC-ALS-DA–SN-MG
	Valid		X	TPC-ALS-245†
	View*Logic*		X	TPC-ALS-DA–SN-VL
HP700	Mentor		X	TPC-ALS-DA-HP7-MG
DN4000/ HP400				TPC-ALS-235†

NOTE 1: Authorization codes for design systems are supplied upon request, after receipt of the system.

† The TPC-ALS-235 and TPC-ALS-245 systems only provide support for the TPC10 and TPC12 series, and will not be supported in Revision 3.0 scheduled for release in the fourth quarter of 1993. These systems are being replaced by TPC-ALS-DA-HP7-MG and TPC-ALS-DA-SN-CD, respectively.

Table 3. TI-ALS Programming Configurations (see Note 2)

HARDWARE PLATFORM	CAE HOST ENVIRONMENT	DESIGN SUPPORT		TI SUSTEM PART NUMBER
		ONE DEVICE	FOUR DEVICES	
386/486-based PC	View*Logic* /OrCAD	X		TPC-ALS-DS–P2S-PC
			X	TPC-ALS-219
Sun	Cadence/Mentor/ Valid/View*Logic*	X		TPC-ALS-DS–P2S-SN
			X	TPC-ALS-249
HP700	Mentor	X		TPC-ALS-DS–P2S-HP7
			X	TPC-ALS-DS–P2-HP7
HP400	Mentor	X		TPC-ALS-DS–P2S-HP4
			X	TPC-ALS-DS–P2-HP4
DN Series	Mentor		X	TPC-ALS-239

NOTE 2: Programming units are compatible with both high (10000 gates) and low (2500 gates) density systems

architecture

device organization

Each FPGA consists of a matrix of logic modules arranged in rows separated by channels containing interconnect tracks. The matrix is surrounded with peripheral inputs, outputs, I/Os, and diagnostic circuits. A partial view of the TPC10 Series logic modules with examples of interconnections is illustrated in Figure 2.

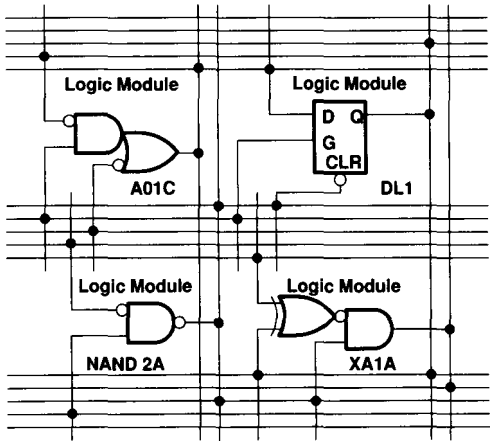

Figure 2. Partial View of TPC10 Series Interconnection Capability

logic module

Each core logic module has the equivalent complexity of four 2-input NAND gates. The module shown in Figure 3, is an 8-input, 1-output gate cluster that can implement hardwired primitive gates, Booleans, latches, flip-flops, multiplexers, half or full adder slices, or multiplexed-input flip-flops. The TI-ALS library contains a full spectrum of 2-, 3-, and 4-input AND, NAND, OR, and NOR gate macros covering all derivatives of true and/or complement input combinations. Similar modular implementations, covering the spectrum of true and/or complement input combinations, are included for each functional category of macros in the library. Latches and flip-flops are created by connecting two or more logic modules in the appropriate circuit configuration. The macros are captured, simulated, placed, analyzed, and programmed using the TPC10 design library.

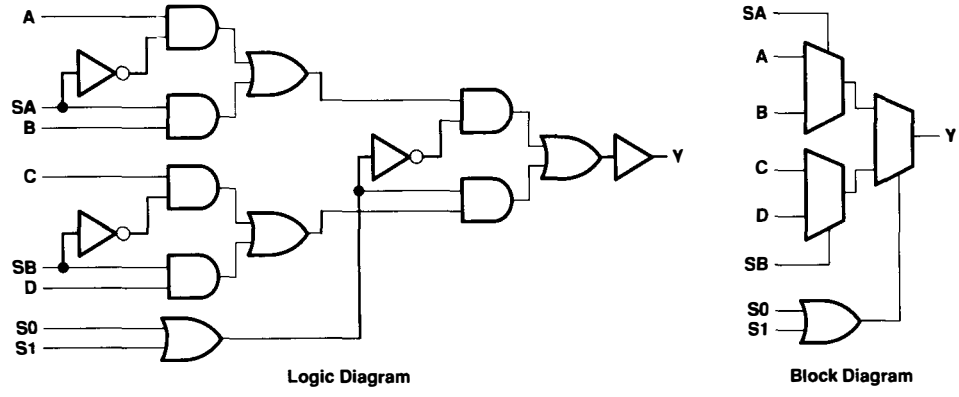

Figure 3. TPC10 Series Logic Module

	TPS73025DBVRG4	23480	新环保批次	SOT23-5
	TPS73028DBVRG4	23480	新环保批次	SOT23-5
	TPS73001DBVRG4	23480	新环保批次	SOT23-6
	TPS73033DBVRG4	23480	新环保批次	SOT23-5
	TPS73018DBVRG4	23480	新环保批次	SOT23-5
	TPS730285DBVRG4	23480	新环保批次	SOT23-5
	TPS7301QDRG4	23480	新环保批次	SOP8
	TPS73025DBVT	23480	新环保批次	SOT23-5
	TPS73025YZQR	23480	新环保批次	DSBGA
	TPS73030DBV	23480	新环保批次	SOT23-5
	TPS73025DBVR.	23480	新环保批次	SOT23-5
	TPS73012DBVR	23480	新环保批次	SOT23-5
	TPS73015DBVR	23480	新环保批次	SOT23-5
	TPS73030DBVTG4	23480	新环保批次	SOT23-5
	TPS73025DBVTG4	23480	新环保批次	SOT23-5
	TPS73028DBVTG4	23480	新环保批次	SOT23-5
	TPS73045DBVR	23480	新环保批次	SOT23-5
	TPS73050DBVR	23480	新环保批次	SOT23-5
	TPS73033DBVTG4	23480	新环保批次	SOT23-5
	BQ24351DSGR	23480	新环保批次	SON-8
	TPS7301QPW	23480	新环保批次	TSSOP
	TPS730285DBV	23480	新环保批次	NA
	TPS73033DBVR.	23480	新环保批次	SOT23-5
	TPS73033DBVR	23480	新环保批次	SOT23-5
	TPS730001DBVR	23480	新环保批次	S0T23
	TPS7301QPWR	23480	新环保批次	TSSOP-20
	TPS73001DBVTG4	23480	新环保批次	
	BQ24105IRHLR	23480	新环保批次	QFN20
	BQ2024DBZRG4	23480	新环保批次	SOT-23
	TPS73033DBVR(PHUI)	23480	新环保批次	SOT23-5
	TPS7301Q	23480	新环保批次	SOP-8
	TPS7301QPWRG4	23480	新环保批次	TSSOP-20