architecture

device organization

Each FPGA consists of a matrix of logic modules arranged in rows separated by channels containing interconnect tracks. The matrix is surrounded with peripheral inputs, outputs, I/Os, and diagnostic circuits. A partial view of the TPC10 Series logic modules with examples of interconnections is illustrated in Figure 2.

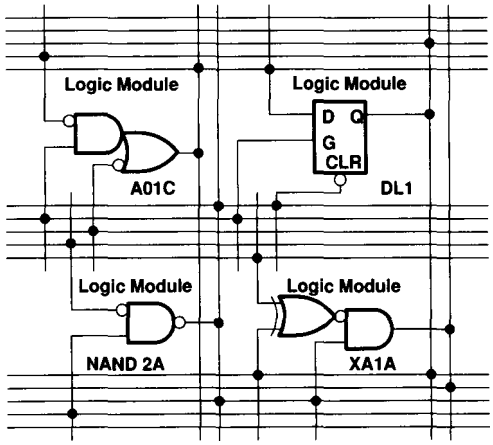

Figure 2. Partial View of TPC10 Series Interconnection Capability

logic module

Each core logic module has the equivalent complexity of four 2-input NAND gates. The module shown in Figure 3, is an 8-input, 1-output gate cluster that can implement hardwired primitive gates, Booleans, latches, flip-flops, multiplexers, half or full adder slices, or multiplexed-input flip-flops. The TI-ALS library contains a full spectrum of 2-, 3-, and 4-input AND, NAND, OR, and NOR gate macros covering all derivatives of true and/or complement input combinations. Similar modular implementations, covering the spectrum of true and/or complement input combinations, are included for each functional category of macros in the library. Latches and flip-flops are created by connecting two or more logic modules in the appropriate circuit configuration. The macros are captured, simulated, placed, analyzed, and programmed using the TPC10 design library.

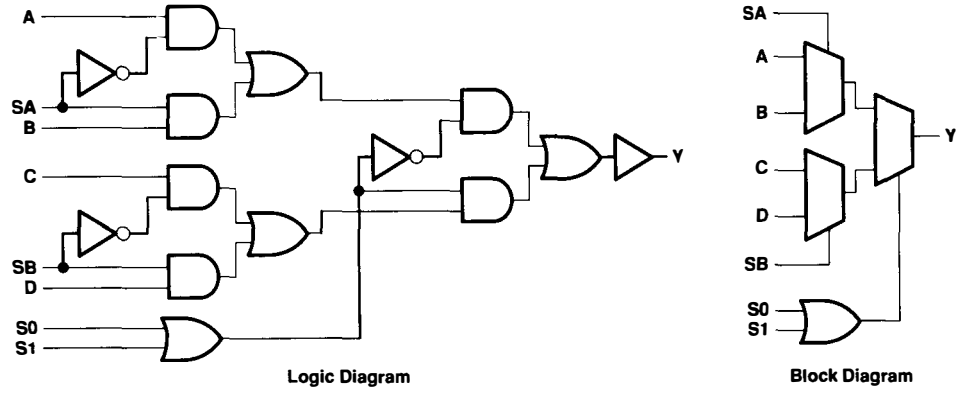

Figure 3. TPC10 Series Logic Module

	TPS73033DBVTG4	23480	新环保批次	SOT23-5
	BQ24351DSGR	23480	新环保批次	SON-8
	TPS7301QPW	23480	新环保批次	TSSOP
	TPS730285DBV	23480	新环保批次	NA
	TPS73033DBVR.	23480	新环保批次	SOT23-5
	TPS73033DBVR	23480	新环保批次	SOT23-5
	TPS730001DBVR	23480	新环保批次	S0T23
	TPS7301QPWR	23480	新环保批次	TSSOP-20
	TPS73001DBVTG4	23480	新环保批次	
	BQ24105IRHLR	23480	新环保批次	QFN20
	BQ2024DBZRG4	23480	新环保批次	SOT-23
	TPS73033DBVR(PHUI)	23480	新环保批次	SOT23-5
	TPS7301Q	23480	新环保批次	SOP-8
	TPS7301QPWRG4	23480	新环保批次	TSSOP-20
	TPS73047DBVT	23480	新环保批次	SOT23-5
	TPS73047DBVTG4	23480	新环保批次	SOT23-5
	BQ27200DRK	23480	新环保批次	QFN18
	BQ2031SN-A5TRG4	23480	新环保批次	SOP16
	TPS73018DBVR TEL	23480	新环保批次	SOT23-5
	TPS73028DBVR TEL	23480	新环保批次	SOT23-5
	TPS73030DBVR TEL	23480	新环保批次	SOT23-5
	TPS73033DBVR TEL	23480	新环保批次	SOT23-5
	TPS730285DBVR TEL	23480	新环保批次	SOT23-5
	TPS73018YZQR TPS73025Y2	23480	新环保批次	
	TPS73028YZQT	23480	新环保批次	SMD
	TPS73033DBVRG4	23480	新环保批次	
	TPS73001DBVRG4	23480	新环保批次	
	TPS73025DBVRG4	23480	新环保批次	
	TPS73030DBVRG4	23480	新环保批次	
	TPS73028DBVRG4	23480	新环保批次	
	TPS73018DBVRG4	23480	新环保批次	
	TPS730285DBVRG4	23480	新环保批次	

interconnect tracks

The channeled interconnect tracks consist of isolated metal segments that can be connected by addressing and programming antifuses. Each channel has 25 horizontal routing tracks, 22 are for logic, one is for clock, one is for power, and one is for ground. In addition, there are 13 vertical routing tracks per logic module column. Both horizontal and vertical tracks, in combination with the approximately 340 antifuses per logic module, produce a network that is capable of interconnecting up to 90 percent of the equivalent gates. Based on the placement of macros, the programming process selects and activates antifuses that both create the logic module macros and I/Os, and interconnect the entire array.

I/O buffers

Each I/O pin is configurable as an input or an output. In addition, I/O pins configured as outputs can be defined as totem-pole, 3-state, or bidirectional. Inputs can be driven by CMOS or TTL levels and output levels are compatible with standard CMOS and TTL specifications. Outputs sink or source a current of 4 mA at TTL output levels. See the dc characteristics for additional I/O buffer specifications. The I/Os can be manually assigned to any available package pin, or the ALS software can automatically place the I/Os in the optimum configuration.

diagnostic probe pins

TPC10 Series devices have two independent diagnostic probe pins, PRA and PRB. The pins allow the user to observe any internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on an oscilloscope, logic analyzer, or with the workstation diagnostics using the Actionprobe diagnostic tools. The probe pins can also be used as user-defined I/Os, depending on the level of the mode control pin. When configured as user-defined I/Os, the pins have the same characteristics as other I/O pins.

security fuses

The TPC10 Series security fuses can be used to permanently disable further diagnostics and testing. After the security fuses are programmed, access to the architecture is not available. This makes the FPGA design difficult to copy.

	TPS730	23480	新环保批次	DSBGASOT-23SOT-23
	BQ2003STR	23480	新环保批次	SOP16
	TPS73030DBVRTI	23480	新环保批次	
	TPS730330DBVR	23480	新环保批次	SOT23-5
	BQ2204ASN-N	23480	新环保批次	SOIC-16
	TPS73028DBV	23480	新环保批次	SOT-23-5
	BQ20z95DBT-V150	23480	新环保批次	TOSSOP44
	TPS73033DBVR	23480	新环保批次	SOT23-5
	TPS73061DBVR	23480	新环保批次	QFN
	BQ29312PWRG4	23480	新环保批次	TSSOP-28
	TPS7301QPWG4	23480	新环保批次	
	TPS7301MJGB	23480	新环保批次	CDIP8
	DAC7311IDCKRG4	23480	新环保批次	ICDAC12-BIT1-CHLPSC7
	BQ25700ARSNT	23480	新环保批次	WQFN32
	BQ29732DSET	23480	新环保批次	
	BQ296203DSGR	23480	新环保批次	
	BQ29312WR-SA	23480	新环保批次	TSSOP-24
	BQ27320YZFR	23480	新环保批次	NA
	BQ27200DRKRG4	23480	新环保批次	
	XLVC14A	23480	新环保批次	SOP-14
	XLVC14AC	23480	新环保批次	SOP-14
	BQ20z45DBT-R0	23480	新环保批次	TOSSOP38
	BQ20z453DBT-R0	23480	新环保批次	TOSSOP38
	BQ29729DSER	23480	新环保批次	WSON6
	BQ29717DSER	23480	新环保批次	WSON6
	LM2775DSGR	23480	新环保批次	WSON8
	LM2775QDSGRQ1	23480	新环保批次	8-WSON
	LM2775QDSGTQ1	23480	新环保批次	8-WSON
	LM2775DSGT	23480	新环保批次	WSON
	LM2775DGST	23480	新环保批次	
	LM2775	23480	新环保批次	
	LM2775 . . .	23480	新环保批次	