Chapter 6

Configuration Details

Configuration Memory Frames

Virtex®-5 FPGA configuration memory is arranged in frames that are tiled about the device. These frames are the smallest addressable segments of the Virtex-5 configuration memory space, and all operations must therefore act upon whole configuration frames. Virtex-5 frame counts and configuration sizes are shown in Table 6-1. Depending on BitGen options, additional overhead exists in the configuration bitstream. The exact bitstream length is available in the rawbits file (.rbt) created by using the "-b" option with bitgen or selecting "Create ASCII Configuration File" in the Generate Programming File options popup in ISE. Bitstream length (words) are roughly equal to the configuration array size (words) plus configuration overhead (words). Bitstream length (bits) are roughly equal to the bitstream length in words times 32.

Table 6-1: **Virtex-5 Device Frame Count, Frame Length, Overhead, and Bitstream Size**

Device	Non-Configuration Frames(1)	Configuration Frames	Total Device Frames	Frame Lengths in Words(2)	Configuration Array Size in Words(3)	Bitstream Overhead in Words(4)
LX30	172	6,376	6,548	41	261,416	272
LX50	258	9,564	9,822	41	392,124	272
LX85	426	16,644	17,070	41	682,404	272
LX110	568	22,192	22,760	41	909,872	272
LX155	800	32,544	33,344	41	1,334,304	272
LX220	1,040	40,496	41,536	41	1,660,336	272
LX330	1,560	60,744	62,304	41	2,490,504	272
LX20T	126	3,762	3,888	41	154,242	272
LX30T	184	7,136	7,320	41	292,576	272
LX50T	276	10,704	10,980	41	438,864	272
LX85T	444	17,784	18,228	41	729,144	272
LX110T	592	23,712	24,304	41	972,192	272
LX155T	808	32,800	33,608	41	1,344,800	272
LX220T	1,064	42,016	43,080	41	1,722,656	272
LX330T	1,596	63,024	64,620	41	2,583,984	272
SX35T	244	10,168	10,412	41	416,888	272
SX50T	366	15,252	15,618	41	625,332	272

Table 6-1: **Virtex-5 Device Frame Count, Frame Length, Overhead, and Bitstream Size *(Continued)***

Device	Non-Configuration Frames(1)	Configuration Frames	Total Device Frames	Frame Lengths in Words(2)	Configuration Array Size in Words(3)	Bitstream Overhead in Words(4)
SX95T	648	27,216	27,864	41	1,115,856	272
SX240T	1,440	60,672	62,112	41	2,487,552	272
FX30T	244	10,296	10,540	41	422,136	272
FX70T	488	20,592	21,080	41	844,272	272
FX100T	696	30,016	30,712	41	1,230,656	272
FX130T	870	37,520	38,390	41	1,538,320	272
FX200T	1,236	54,000	55,236	41	2,214,000	272
TX150T	810	32,980	33,790	41	1,352,180	272
TX240T	1,236	50,112	51,348	41	2,054,592	272

1. Non-configuration frames do not contribute to the bitstream size.
2. All Virtex-5 configuration frames consist of 41 32-bit words.
3. Configuration array size equals the number of configuration frames times the number of words per frame.
4. Configuration overhead consists of commands in the bitstream that are needed to perform configuration but do not themselves program any memory cells. Configuration overhead contributes to the overall bitstream size.

Configuration Registers

All Virtex-5 FPGA bitstream commands are executed by reading or writing to the configuration registers.

Packet Types

The FPGA bitstream consists of two packet types: Type 1 and Type 2. These packet types and their usage are described below.

Type 1 Packet

The Type 1 packet is used for register reads and writes. Only 5 out of 14 register address bits are used in Virtex-5 FPGAs. The header section is always a 32-bit word.

Following the Type 1 packet header is the Type 1 Data section, which contains the number of 32-bit words specified by the word count portion of the header.

Table 6-2: **Type 1 Packet Header Format**

Header Type	Opcode	Register Address	Reserved	Word Count
[31:29]	[28:27]	[26:13]	[12:11]	[10:0]
001	xx	RRRRRRRRRxxxxx	RR	xxxxxxxxxxx

Notes:

1. "R" means the bit is not used and reserved for future use.

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Virtex-II Pro	☐
系列:	XC2VP30	☐
逻辑元件数量:	30816 LE	☐
自适应逻辑模块 - ALM:	13696 ALM	☐
嵌入式内存:	2.39 Mbit	☐
输入/输出端数量:	664 I/O	☐
工作电源电压:	1.5 V	☐
最小工作温度:	- 40 C	☐
最大工作温度:	+ 100 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-1152	☐
数据速率:	6.25 Gb/s	
商标:	Xilinx	
分布式RAM:	428 kbit	
内嵌式块RAM - EBR:	2448 kbit	
最大工作频率:	350 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	3424 LAB	
收发器数量:	8 Transceiver	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	1	
子类别:	Programmable Logic ICs	
商标名:	Virtex	

Readback Capture

The configuration memory readback command sequence is identical for both Readback Verify and Readback Capture. However, the Capture sequence requires an additional step to sample internal register values.

Users can sample block RAM outputs, and CLB and IOB registers by instantiating the CAPTURE_VIRTEX5 primitive in their design (Figure 7-7) and asserting the CAP input on that primitive while the design is operating. On the next rising clock edge on the CAPTURE_VIRTEX5 CLK input, the internal GRDBK signal is asserted, storing all CLB and IOB register values into configuration memory cells. These values can then be read out of the device along with the IOB and CLB configuration columns by reading configuration memory through the readback process. Register values are stored in the same memory cell that programs the register's init state configuration, thus sending the GRESTORE command to the Virtex-5 configuration logic after the Capture sequence can cause registers to return to an unintended state.

Alternatively, the GRDBK signal can be asserted by writing the GCAPTURE command to the CMD register. This command asserts the GRDBK signal for two CCLK or TCK cycles, depending on the startup clock setting.

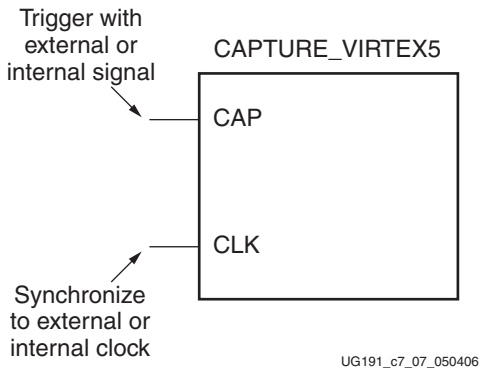

Figure 7-7: **Virtex-5 Device Library Primitive**

Table 7-8: **Capture Signals**

Signal	Description	Access
GCAPTURE	Captures the state of all slice and IOB registers. Complement of GRESTORE.	GCAPTURE command through the CMD register or *CAP* input on capture block, user controlled.
GRESTORE	Initializes all registers as configured.	CMD register and STARTUP_VIRTEX5 block.

If the CAP signal is left asserted over multiple clock cycles, the Capture cell is updated with the new register value on each rising clock edge. To limit the capture operation to the first rising clock edge, the user can add the ONESHOT attribute to the CAPTURE_VIRTEX5 primitive. More information on the ONESHOT attribute can be found in the Constraints Guide.

Once the configuration memory frames have been read out of the device, the user can pick the captured register values out of the readback data stream. The capture bit locations are given in the logic allocation file (`design.ll`) as described in Table 7-9.

芯片详细信息

Manufacturer Part Number: XC2VP30-6FFG1152I	Pbfree Code: Yes	Rohs Code: Yes	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA1152,34X34,40	Pin Count: 1152
Reach Compliance Code: not_compliant	ECCN Code: 3A991.D	HTS Code: 8542.39.00.01	Manufacturer: Xilinx
Risk Rank: 5.78	Clock Frequency-Max: 1200 MHz	Combinatorial Delay of a CLB-Max: 0.32 ns	JESD-30 Code: S-PBGA-B1152
JESD-609 Code: e1	Length: 35 mm	Moisture Sensitivity Level: 4	Number of CLBs: 3424
Number of Inputs: 644	Number of Logic Cells: 30816	Number of Outputs: 644	Number of Terminals: 1152
Organization: 3424 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA1152,34X34,40
Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 245	Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.4 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V	Surface Mount: YES
Technology: CMOS	Terminal Finish: Tin/Silver/Copper (Sn95.5Ag4.0Cu0.5)	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 35 mm	