*Table 1-29:* **Onboard Power System Devices *(Cont'd)***

| Device Type | Reference Designator | Description | Power Rail Net Name | Power Rail Voltage | Schematic Page |
|---|---|---|---|---|---|
| TPS51200DR | U33 | Tracking Regulator, 3A | VTTDDR | 0.75V | 46 |

**Notes:**
1. See Table 1-30.
2. See Table 1-31.
3. See Table 1-34.

Data sheets for the Texas Instruments controller and regulators are available at the Texas Instruments website [Ref 25], and for the Analog Devices ADP123 at [Ref 26].

## FMC_VADJ Voltage Control

The FMC_VADJ rail is set to 1.8V. When the VC707 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J51 is sampled by the TI UCD9248 controller U42. If a jumper is installed on J51 signal FMC_VADJ_ON_B is held low, and the TI controller U42 energizes the FMC_VADJ rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J51 jumper, removing the jumper at J51 after the board is powered up does not affect the 1.8V power delivered to the FMC_VADJ rail and it remains on.

A jumper installed at J51 is the default setting.

If a jumper is not installed on J51, signal FMC_VADJ_ON_B is high, and the VC707 board does not energize the FMC_VADJ 1.8V at power on. In this mode the user can control when to turn on FMC_VADJ and to what voltage level (1.2V, 1.5V, 1.8V). With FMC_VADJ off, the FPGA still configures and has access to the TI controller PMBUS along with the VADJ_ON_B signal. The combination of these allows the user to develop code to command the FMC_VADJ rail to be set to something other than the default setting of 1.8V. After the new FMC_VADJ voltage level has been programmed into TI controller U42, the VADJ_ON_B signal can be driven low by the user logic and the FMC_VADJ rail comes up at the new FMC_VADJ voltage level. Installing a jumper at J51 after a VC707 board powers up in this mode turns on the FMC_VADJ rail.

Documentation describing PMBUS programming for the UCD9248 digital power controller is available at the Texas Instruments website [Ref 25].

## Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface. The three onboard TI power controllers (U42 at address 52, U43 at address 53, and U64 at address 54) are wired to the same PMBus. The PMBus connector, J5, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO), which can be ordered from the TI website [Ref 25], and the associated TI Fusion Digital Power Designer GUI (downloadable from [Ref 25]). This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-30, Table 1-31, and Table 1-32.

In each of these the three tables (one per controller), the Power Good (PG) On Threshold is the set-point at or above which the particular rail is deemed "good". The PG Off Threshold is the set-point at or below which the particular rail is no longer deemed "good". The controller internally OR's these PG conditions together and drives an output PG pin high only if all active rail PG states are "good". The On and Off Delay and rise and fall times are relative to when the board power on-off slide switch SW12 is turned on and off.

Table 1-30 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 52 (U42).

*Table 1-30:* **Power Rail Specifications for UCD9248 PMBus Controller at Address 52**

| Rail Number | Rail Name | Schematic Rail Name | Nominal $V_{OUT}$ (V) | PG On Threshold (V) | PG Off Threshold (V) | On Delay (ms) | Rise Time (ms) | Off Delay (ms) | Fall Time (ms) | Shutdown Threshold[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $V_{OUT}$ Over Fault (V) | $I_{OUT}$ Over Fault (A) | Temp Over Fault (°C) |
| 1 | Rail #1 | VCCINT_FPGA | 1 | 0.9 | 0.85 | 0 | 5 | 10 | 1 | 1.15 | 20 | 90 |
| 2 | Rail #2 | VCCAUX | 1.8 | 1.62 | 1.53 | 0 | 5 | 5 | 1 | 2.07 | 10.41 | 90 |
| 3 | Rail #3 | VCC3V3 | 3.3 | 2.97 | 2.805 | 0 | 5 | 4 | 1 | 3.795 | 10.41 | 90 |
| 4 | Rail #4 | VADJ | 1.8 | 1.62 | 1.53 | 0 | 5 | 3 | 1 | 2.07 | 10.41 | 90 |

**Notes:**

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

Table 1-31 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 53 (U43).

*Table 1-31:* **Power Rail Specifications for UCD9248 PMBus Controller at Address 53**

| Rail Number | Rail Name | Schematic Rail Name | Nominal $V_{OUT}$ (V) | PG On Threshold (V) | PG Off Threshold (V) | On Delay (ms) | Rise Time (ms) | Off Delay (ms) | Fall Time (ms) | Shutdown Threshold[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $V_{OUT}$ Over Fault (V) | $I_{OUT}$ Over Fault (A) | Temp Over Fault (°C) |
| 1 | Rail #1 | VCC2V5_FPGA | 2.5 | 2.25 | 2.125 | 0 | 5 | 1 | 1 | 2.875 | 10.41 | 90 |
| 2 | Rail #2 | VCC1V5 | 1.5 | 1.35 | 1.275 | 0 | 5 | 0 | 1 | 1.725 | 10.41 | 90 |
| 3 | Rail #3 | MGTAVCC | 1 | 0.9 | 0.85 | 0 | 5 | 7 | 1 | 1.45 | 10.41 | 90 |
| 4 | Rail #4 | MGTAVTT | 1.2 | 1.08 | 1.02 | 0 | 5 | 8 | 1 | 1.38 | 10.41 | 90 |

**Notes:**

1. The values defined in these columns are the voltage, current, and temperature thresholds that causes the regulator to shut down if the value is exceeded.

Table 1-32 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 54 (U64).

*Table 1-32:* **Power Rail Specifications for UCD9248 PMBus Controller at Address 54**

| Rail Number | Rail Name | Schematic Rail Name | Nominal $V_{OUT}$ (V) | PG On Threshold (V) | PG Off Threshold (V) | On Delay (ms) | Rise Time (ms) | Off Delay (ms) | Fall Time (ms) | Shutdown Threshold[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $V_{OUT}$ Over Fault (V) | $I_{OUT}$ Over Fault (A) | Temp Over Fault (°C) |
| 1 | Rail #1 | VCCAUX_IO | 2 | 1.8 | 1.7 | 0 | 5 | 2 | 1 | 2.3 | 10.41 | 90 |
| 2 | Rail #2 | VCC_BRAM | 1 | 0.9 | 0.85 | 0 | 5 | 9 | 1 | 1.15 | 10.41 | 90 |
| 3 | Rail #3 | MGTVCCAUX | 1.8 | 1.62 | 1.53 | 0 | 5 | 7 | 1 | 2.07 | 10.41 | 90 |
| 4 | Rail #4 | VCC1V8_FPGA | 1.8 | 1.62 | 1.53 | 0 | 5 | 5 | 1 | 2.07 | 10.41 | 90 |

**Notes:**

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

## FPGA Cooling Fan Operation

The FPGA cooling fan control circuit has its PWM signal wired to a dual-use FPGA Bank 15 pin BA37. After configuration, this pin is expected to be toggled by user-provided fan speed control IP to control fan speed.

FPGA U1 pin BA37 is alternately an unused BPI flash memory address pin (A28). During FPGA configuration in BPI mode, the BPI flash memory address lines are driven. The BA37 pin is held low during BPI configuration and thus the fan PWM signal is not active. The FPGA U1 cooling fan is off during the FPGA BPI configuration process.

After configuration is complete, the dual-use FPGA pin BA37 is available for use by user-provided fan speed control IP.

## References

More information about the power system components used by the VC707 board are available from the Texas Instruments digital power website [Ref 25].

## PCIe Form Factor Board TI Power System Cooling

If the power modules on the VC707 board are operating at moderate to high current levels (due to a customer design), the modules can generate substantial heat, which can cause them to shut down without warning. The power module shutdown then turns off the FPGA on the development board. Refer to the Virtex-7 FPGA VC707 Evaluation Kit Master Answer Record in Appendix G: References for more information.

芯片详细信息

| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>XC2VP30-6FF896I | Pbfree Code:<br>No | Rohs Code:<br>No | Part Life Cycle Code:<br>Obsolete |
| Ihs Manufacturer:<br>XILINX INC | Part Package Code:<br>BGA | Package Description:<br>BGA, BGA896,30X30,40 | Pin Count:<br>896 |
| Reach Compliance Code:<br>not_compliant | ECCN Code:<br>3A991.D | HTS Code:<br>8542.39.00.01 | Manufacturer:<br>Xilinx |
| Risk Rank:<br>5.8 | Clock Frequency-Max:<br>1200 MHz | Combinatorial Delay of a CLB-Max:<br>0.32 ns | JESD-30 Code:<br>S-PBGA-B896 |
| JESD-609 Code:<br>e0 | Length:<br>31 mm | Moisture Sensitivity Level:<br>4 | Number of CLBs:<br>3424 |
| Number of Inputs:<br>556 | Number of Logic Cells:<br>30816 | Number of Outputs:<br>556 | Number of Terminals:<br>896 |
| Organization:<br>3424 CLBS | Package Body Material:<br>PLASTIC/EPOXY | Package Code:<br>BGA | Package Equivalence Code:<br>BGA896,30X30,40 |
| Package Shape:<br>SQUARE | Package Style:<br>GRID ARRAY | Peak Reflow Temperature (Cel):<br>225 | Power Supplies:<br>1.5,1.5/3.3,2/2.5,2.5 V |
| Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY | Qualification Status:<br>Not Qualified | Seated Height-Max:<br>3.4 mm | Subcategory:<br>Field Programmable Gate Arrays |
| Supply Voltage-Max:<br>1.575 V | Supply Voltage-Min:<br>1.425 V | Supply Voltage-Nom:<br>1.5 V | Surface Mount:<br>YES |
| Technology:<br>CMOS | Terminal Finish:<br>Tin/Lead (Sn63Pb37) | Terminal Form:<br>BALL | Terminal Pitch:<br>1 mm |
| Terminal Position:<br>BOTTOM | Time@Peak Reflow Temperature-Max (s):<br>30 | Width:<br>31 mm | |

| | | |
|---|---|---|
| 产品种类: | FPGA - 现场可编程门阵列 | ☑ |
| 产品: | Virtex-II Pro | ☐ |
| 系列: | XC2VP30 | ☐ |
| 逻辑元件数量: | 30816 LE | ☐ |
| 自适应逻辑模块 - ALM: | 13696 ALM | ☐ |
| 嵌入式内存: | 2.39 Mbit | ☐ |
| 输入/输出端数量: | 556 I/O | ☐ |
| 工作电源电压: | 1.5 V | ☐ |
| 最小工作温度: | - 40 C | ☐ |
| 最大工作温度: | + 100 C | ☐ |
| 安装风格: | SMD/SMT | ☐ |
| 封装 / 箱体: | FBGA-896 | ☐ |
| 数据速率: | 6.25 Gb/s | |
| 商标: | Xilinx | |
| 分布式RAM: | 428 kbit | |
| 内嵌式块RAM - EBR: | 2448 kbit | |
| 最大工作频率: | 350 MHz | |
| 湿度敏感性: | Yes | |
| 逻辑数组块数量——LAB: | 3424 LAB | |
| 收发器数量: | 8 Transceiver | |
| 产品类型: | FPGA - Field Programmable Gate Array | |
| 工厂包装数量: | 1 | |
| 子类别: | Programmable Logic ICs | |
| 商标名: | Virtex | |