TX PRBS Generator

Overview

Pseudo-random bit sequences (PRBS) are commonly used to test the signal integrity of high-speed links. These sequences appear random but have specific properties that can be used to measure the quality of a link.

The GTX PRBS block can generate several industry-standard PRBS patterns. Table 6-13 lists the available PRBS patterns and their typical uses.

Table 6-13: **Pseudo-Random Bit Sequences**

Name	Polynomial	Length of Sequence (bits)	Consecutive Zeros	Typical Use
PRBS-7	$1 + X^6 + X^7$ (inverted)	$2^7 - 1$	7	Used to test channels with 8B/10B.
PRBS-23	$1 + X^{18} + X^{23}$ (inverted)	$2^{23} - 1$	23	ITU-T Recommendation O.150, Section 5.6. One of the recommended test patterns in the SONET specification.
PRBS-31	$1 + X^{28} + X^{31}$ (inverted)	$2^{31} - 1$	31	ITU-T Recommendation O.150, Section 5.8. A recommended PRBS test pattern for 10 Gigabit Ethernet. See IEEE 802.3ae-2002.

Ports and Attributes

Table 6-14 defines the TX PRBS generator ports.

Table 6-14: **TX PRBS Generator Ports**

Port	Direction	Clock Domain	Description
TXENPRBSTST0[1:0] TXENPRBSTST1[1:0]	In	TXUSRCLK2	Transmitter test pattern generation control. A pseudo-random bit sequence (PRBS) is generated by enabling the test pattern generation circuit. `00`: Test pattern generation off (standard operation mode) `01`: Enable $2^7 - 1$ PRBS generation `10`: Enable $2^{23} - 1$ PRBS generation `11`: Enable $2^{31} - 1$ PRBS generation Because PRBS patterns are deterministic, the receiver can check the received data against a sequence of its own PRBS generator.

There are no attributes in this section.

Description

Each GTX transceiver includes a built-in PRBS generator. This feature can be used in conjunction with other test features, such as loopback and the built-in PRBS checker, to run tests on a given channel.

To use the PRBS generator, the PRBS test mode is selected using the TXENPRBSTST port. Table 6-14 lists the available settings.

Parallel In to Serial Out

Overview

The Parallel In to Serial Out (PISO) block is the heart of the GTX TX datapath. It serializes parallel data from the PCS using a high-speed clock from the shared PMA PLL.

The PISO block serializes 16 or 20 bits per parallel clock cycle, depending on the internal data width for the tile (INTDATAWIDTH). The clock rate is determined by the shared PMA PLL rate, divided by a local TX divider.

Ports and Attributes

Table 6-15 defines the TX PISO ports.

Table 6-15: **TX PISO Ports**

Port	Direction	Clock Domain	Description
INTDATAWIDTH	In	Async	Specifies the width of the internal datapath for the entire GTX_DUAL tile. This shared port is also described in "Shared PMA PLL," page 86. 0: Internal datapath is 16 bits wide 1: Internal datapath is 20 bits wide

Table 6-16 defines the TX PISO attributes.

Table 6-16: **TX PISO Attributes**

Attribute	Type	Description
OVERSAMPLE_MODE	Boolean	This shared attribute activates the built-in 5x digital oversampling circuits in both GTX transceivers. Oversampling must be enabled when running the GTX transceivers at line rates between 150 Mb/s and 750 Mb/s. TRUE: Built-in 5x digital oversampling enabled for both GTX transceivers on the tile FALSE: Digital oversampling disabled See "Oversampling," page 185 for more details about 5x digital oversampling.
PLL_TXDIVSEL_OUT_0 PLL_TXDIVSEL_OUT_1	Integer	Sets the divider for the TX line rate for the individual GTX transceiver. The divider can be set to 1, 2, or 4.

Description

Equation 6-5 shows how to calculate the TX line rate when operating without oversampling (OVERSAMPLE_MODE = FALSE).

$$\text{Tx Line Rate} = \frac{\text{PLL Clock Rate} \times 2}{\text{PLL\_TXDIVSEL\_OUT}} \quad \textit{Equation 6-5}$$

When oversampling is activated, use Equation 6-6 to calculate the line rate.

$$\text{Tx Line Rate} = \frac{\text{PLL Clock Rate} \times 2}{\text{PLL\_TXDIVSEL\_OUT} \times 5} \quad \textit{Equation 6-6}$$

See "Oversampling," page 185 for more information about oversampling.

芯片详细信息

Manufacturer Part Number: XC2VP30-5FG676C	Pbfree Code: No	Rohs Code: No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA676,26X26,40	Pin Count: 676
Reach Compliance Code: not_compliant	ECCN Code: 3A991.D	HTS Code: 8542.39.00.01	Manufacturer: Xilinx
Risk Rank: 8.74	Clock Frequency-Max: 1050 MHz	Combinatorial Delay of a CLB-Max: 0.36 ns	JESD-30 Code: S-PBGA-B676
JESD-609 Code: e0	Length: 27 mm	Moisture Sensitivity Level: 3	Number of CLBs: 3424
Number of Inputs: 416	Number of Logic Cells: 30816	Number of Outputs: 416	Number of Terminals: 676
Operating Temperature-Max: 85 °C	Organization: 3424 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA676,26X26,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 225
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.44 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V	Surface Mount: YES
Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: Tin/Lead (Sn63Pb37)	Terminal Form: BALL
Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 27 mm

XC3090A-3PQ208C	2001+	qfp	2315
XC3090A-3PQ160C	2001+	QFP	2315
XC3090A-3PQ160	2001+	QFP	2315
XC3090A-100PG175I	2001+	PGA	2315
XC3090A-100PG175C	2001+	BGA	2315
XC3090A-007PC84	2001+	BGA	2315
XC3090A	2001+	PLCC84	2315
XC3090-7PQ160I	2001+	QFP	2315
XC3090-7-PQ160C	2001+	QFPBGAPLCC	2315
XC3090-7PQ160C	2001+	QFP	2315
XC3090-7PC84I	2001+	PLCC	2315
XC3090-7PC84C	2001+	PLCC84	2315
XC3090-70PQ208	2001+	QFP	2315
XC3090-70PQ160I	2001+	QFP160	2315
XC3090-70PQ160C	2001+	QFP160	2315
XC3090-70PQ160	2001+	QFP	2315
XC3090-70PP175I	2001+	原厂原封	2315
XC3090-70PP175C0236	2001+	PGA	2315
XC3090-70PP175C	2001+	BGA	2315
XC3090-70PG175M	2001+	BGA	2315
XC3090-70PG175I	2001+	原厂原封	2315
XC3090-70PG175CX	2001+	PGA	2315
XC3090-70PG175C	2001+	DIP	2315
XC3090-70PG175B	2001+	PGA	2315
XC3090-70PG175	2001+	BGA	2315
xc3090-70pg	2001+	BGA	2315
XC3090-70PC84I	2001+	原厂原封	2315
XC3090-70PC84C0100	2001+	BGA	2315
XC3090-70PC-84C	2001+	PLCC84	2315
XC3090-70PC84C	2001+	PLCC	2315
XC3090-70PC84	2001+	原厂原封	2315
XC3090-70PC68C	2001+	PLCC	2315
XC3090-70PC68	2001+	plcc	2315
XC3090-70PC100C	2001+	QFP	2315
XC3090-70OG175B	2001+	PGA	2315
XC3090-70CPQ160	2001+	BGA	2315
XC3090-70CB164B	2001+	QFP	2315
XC3090-70APQ208I	2001+	BGA	2315
XC3090-70APQ208	2001+	BGA	2315
XC3090-70/PP175C	2001+	BULKPGA	2315
XC3090-70 PC84	2001+	PLCC	2315

In most chip-to-chip applications operating at 5 Gb/s with up to a nominal trace length of 48 inches with approximately 15.5 dB of attenuation at 2.5 GHz, RX linear equalization with a slight boost on DFETAP1 is sufficient. TX pre-emphasis can also reduce ISI and replace the function of DFE.

Table 7-9 provides DFETAP1 and RXEQMIX settings for 6.5 Gb/s operation for chip-to-chip applications.

Table 7-9: **DFETAP1 and RXEQMIX at 6.5 Gb/s for Chip-to-Chip Applications**

Nominal Trace Length on FR4 Substrate (inches [mm])	Loss (dB) @ 3.25 GHz	DFETAP1	
		RXEQMIX = 10	RXEQMIX = 00
18 [457.2]	8	10	5
28 [711.2]	11.5	31	5
38 [965.2]	15.5	N/A	25
48 [1219.2]	20	N/A	31

Notes:

1. GTX TXDIFFCTRL = `111` and TXPREEMPHASIS = `000` (maximum TX swing and no TX pre-emphasis).

In most chip-to-chip applications, where the nominal trace length is 10 inches and shorter at 6.5 Gb/s, TX pre-emphasis and continuous time linear equalization are sufficient. For longer chip-to-chip applications, the DFE should be used.

Example RX Linear Equalizer and DFE Settings for Backplane Applications

Table 7-10 provides DFETAP1 and RXEQMIX settings for 4.25 Gb/s operation for backplane applications.

Table 7-10: **DFETAP1 and RXEQMIX at 4.25 Gb/s for Backplane Applications**

Nominal Trace Length on FR4 Substrate (inches [mm])	Loss (dB) @ 2.125 GHz	DFETAP1	
		RXEQMIX = 10	RXEQMIX = 00
30 [762](2)	7.75 - 8.25	5	0
44 [1117.6](3)	9.5 - 11	N/A	0
64 [1625.6](4)	13.5 - 17	N/A	23

Notes:

1. GTX TXDIFFCTRL = `111` and TXPREEMPHASIS = `000` (maximum TX swing and no TX pre-emphasis).
2. Nominal 30 inches [762 mm] trace length = 6 inches [152.4 mm] backplane + 2 HmZD or eHSD connectors (trace length neglected) + 24 inches [609.6 mm] on line cards.
3. Nominal 44 inches [1117.6 mm] trace length = 20 inches [508 mm] backplane + 2 HmZD or eHSD connectors (trace length neglected) + 24 inches [609.6 mm] on line cards.
4. Nominal 64 inches [1625.6 mm] trace length = 40 inches [1016 mm] backplane + 2 HmZD or eHSD connectors (trace length neglected) + 24 inches [609.6 mm] on line cards.

In most backplane applications operating at 4.25 Gb/s with up to a total nominal trace length of 64 inches and an end-to-end attenuation of 17 dB at 2.125 GHz, RX linear equalization alone is sufficient.