The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (renwe, address, byte enable, datain, and output registers). Only the output register can be bypassed. The six labclk signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the clock_a, clock_b, renwe_a, renwe_b, clr_a, clr_b, clocken_a, and clocken_b signals, as shown in Figure 2–21.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–22 shows the M4K RAM block to logic array interface.

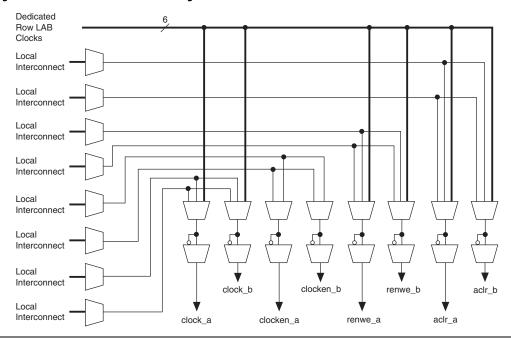


Figure 2-21. M4K RAM Block Control Signals

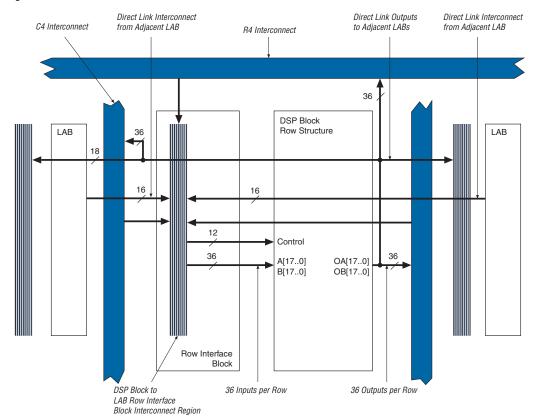


Figure 2-30. DSP Block Interface to Interconnect

A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed/unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface.

EP4SGX180KF40C4N	[48	BGA	20+	ALTERA
EP4SGX180KF40I3N	62	BGA	20+	Intel/Altera
EP4SGX180KF40I4N	3197	BGA	20+	ALTERA
EP4SGX230FF35C3N	155	FCBGA1136	20+	ALTERA
EP4SGX230FF35C3N	50	BGA	20+	ALTERA
EP4SGX230FF35C4N	185	BGA	20+	ALTERA
EP4SGX230FF35I3N	120	BGA	20+	ALTERA
EP4SGX230FF35I3N	[101	BGA	20+	ALTERA
EP4SGX230FF35I4N	500	BGA	20+	ALTERA
EP4SGX230FF35I4N	100	BGA	20+	ALTERA
EP4SGX230HF35C2N	152	BGA	20+	ALTERA
EP4SGX230HF35I3N	160	BGA	20+	ALTERA
EP4SGX230HF35I4N	72	BGA	20+	ALTERA
EP4SGX230KF40C2N	280	BGA	20+	ALTERA
EP4SGX230KF40C3N	280	BGA	20+	ALTERA
EP4SGX230KF40C4N	145	BGA	20+	ALTERA
EP4SGX230KF40C4N	58	BGA	20+	Intel/Altera
EP4SGX230KF40I3N	180	BGA	20+	ALTERA
EP4SGX230KF40I3N	840	BGA	20+	ALTERA
EP4SGX230KF40I4N	277	BGA2397	20+	XILINX
EP4SGX230KF40I4N	231	FCBGA900	20+	ALTERA
EP4SGX290KF40C2N	2000	BGA	20+	ALTERA
EP4SGX290KF40C3N	42000	SOT-353	20+	ALTERA
EP4SGX290NF4513N	280	BGA	20+	ALTERA
EP4SGX360FF35C3N	1000	BGA	20+	ALTERA
EP4SGX360FF35C4N	25	BGA	20+	ALTERA
EP4SGX360FF35I4N	500	DIP	20+	ALTERA
EP4SGX360FH29C3N	[178	BGA	20+	ALTERA
EP4SGX360HF35C2N	200	QFN64	20+	ALTERA
EP4SGX360HF35C3N	50	BGA	20+	ALTERA
EP4SGX360HF35C4N	2000	BGA64	20+	ALTERA
EP4SGX360HF35I3N	184	DIP-4	20+	ALTERA
EP4SGX360HF35I4N	2900	TSSOP24	20+	ALTERA
EP4SGX360KF40C2N	68	BGA	20+	ALTERA
EP4SGX360KF40C3N	7 2	BGA	20+	ALTERA
EP4SGX360KF40C4N	[102	FBGA1152	20+	ALTERA
EP4SGX360KF40I3N	120	FBGA1158	20+	ALTERA

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EP2AGX260FF35I3N	263	FCBGA676	20+	ALTERA
EP2AGX260FF35I5N	165	BGA	20+	ALTERA
EP2AGX45CU17C4N	50	BGA	20+	ALTERA
EP2AGX45CU17I3G	50	BGA	20+	ALTERA
EP2AGX45DF25I3N	100	FBGA1156	20+	ALTERA
EP2AGX45DF29C5N	293	FCBGA1152	20+	ALTERA
EP2AGX45DF29I3N	167	FBGA1156	20+	ALTERA
EP2AGX65DF25C6N	263	FCBGA1738	20+	ALTERA
EP2AGX65DF25I3N	500	BGA900	20+	ALTERA
EP2AGX65DF25I5N	190	BGA2397	20+	XILINX
EP2AGX65DF25I5N	120	FBGA	20+	ALTERA
EP2AGX65DF29C4N	120	FBGA	20+	ALTERA
EP2AGX65DF29C5N	45	BGA	20+	ALTERA
EP2AGX65DF29C6N	116	FCBGA1517	20+	ALTERA
EP2AGX65DF29I3N	60	BGA	20+	Intel/Altera
EP2AGX65DF29I3N	133	FCBGA1517	20+	ALTERA
EP2AGX65DF29I5N	172	BGA	20+	ALTERA
EP2AGX95DF25C4N	200	FCBGA	20+	ALTERA
EP2AGX95DF25C6N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I5N	58	FPBGA1020	20+	ALTERA
EP2AGX95EF29C4N	1080	BGA	20+	ALTERA
EP2AGX95EF29C5N	50	BGA	20+	Intel/Altera
EP2AGX95EF29C5N	50	BGA	20+	ALTERA
EP2AGX95EF29C6N	15	BGA	20+	ALTERA
EP2AGX95EF29I3N	72	FBGA1156	20+	ALTERA
EP2AGX95EF35C6N	455	FBGA1152	20+	ALTERA
EP2AGX95EF35I3N	400	DIP	20+	ALTERA
EP2AGX95EF35I5N	426	BGA1152	20+	ALTERA
EP2AGZ300FF35I3N	500	T0220-7	20+	ALTERA
EP2AGZ300FH29I3N	4000	DIP16	20+	ALTERA
EP2AGZ300HF40I3N	1400	SOP	20+	ALTERA
EP2AGZ300HF40I4N	1500	PWRSO-10	20+	ALTERA
EP2AGZ350FF35I3N	50	BGA	20+	ALTERA
EP2AGZ350FF35I4N	14000	TSSOP20	20+	ALTERA
EP2AGZ350FH29I3N	350	S0T233	20+	ALTERA

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.



For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	√ (1)	√ (1)	✓
	Enhanced configuration device		√ (2)	✓
AS	Serial configuration device	✓	✓	√ (3)
	MAX II device or microprocessor and flash device	✓	~	✓
	Enhanced configuration device	✓	✓	✓
	Download cable (4)	✓	✓	