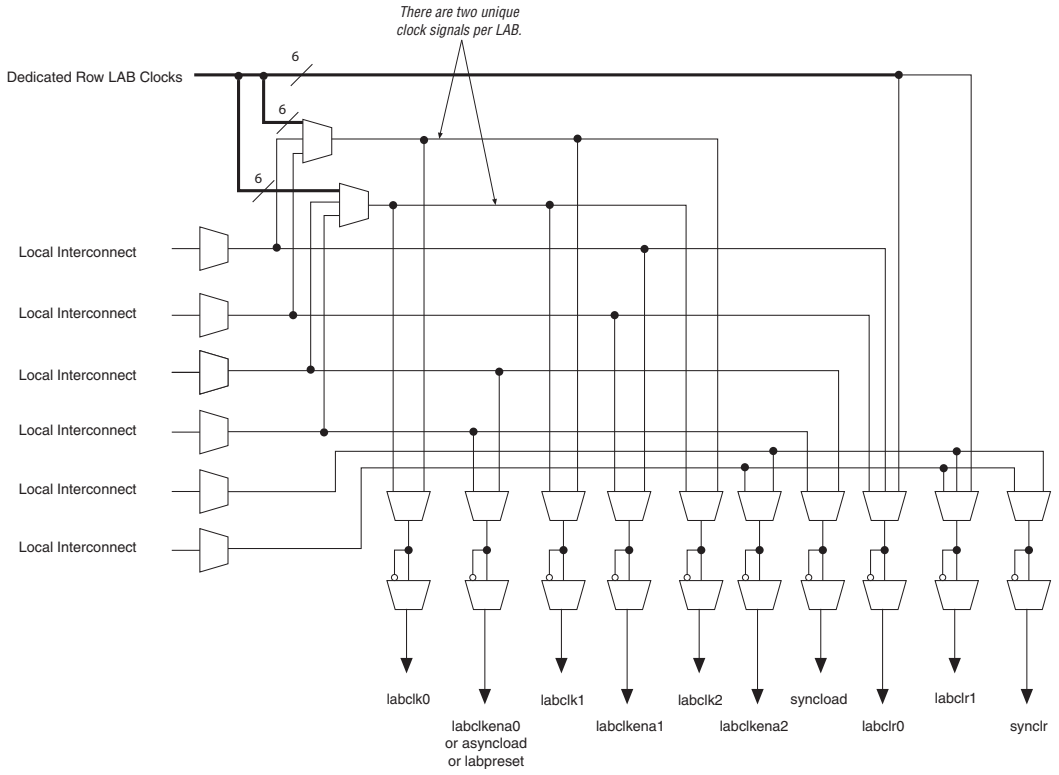
load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–34 shows the LAB control signal generation circuit.

Figure 2–34. LAB-Wide Control Signals

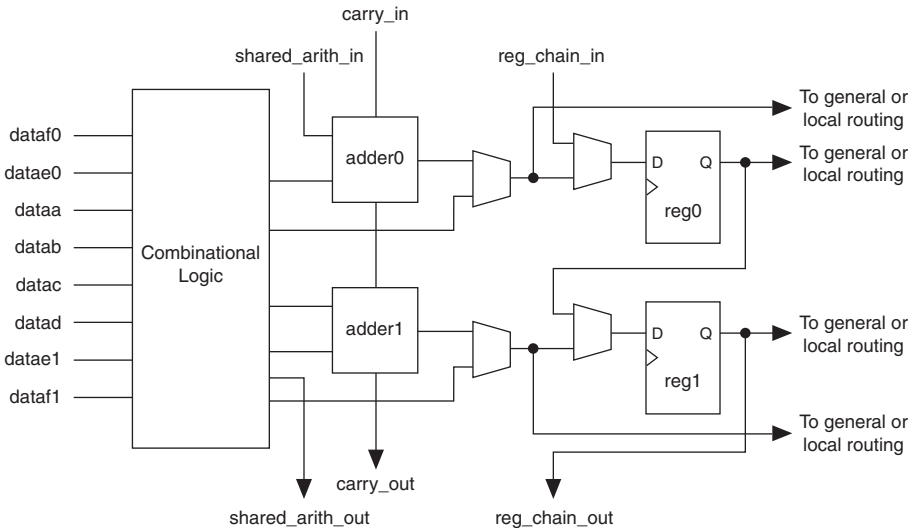


Adaptive Logic Modules

The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

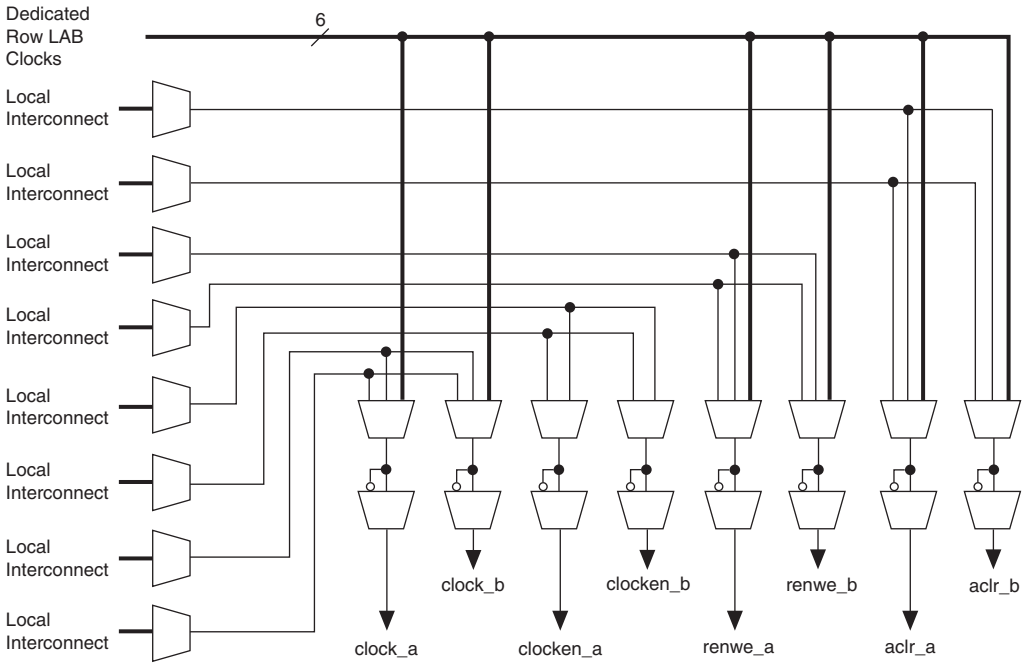
Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM



5SGXEA7K2F40I3N	100	BGA	20+	ALTERA
5SGXEA7K2F40I4N	294	BGA	20+	ALTERA
5SGXEA7N2F45C2N	256	BGA	20+	ALTERA
5SGXEA7N2F45I3N	42	BGA	20+	ALTERA
5SGXMA3H2F35I3N	10000	QFP	20+	ALTERA
5SGXMA4H2F35I3N	280	BGA	20+	ALTERA
5SGXMA5N2F45C2N	111	BGA	20+	ALTERA
5SGXMA5N2F45I3N	124	BGA	20+	ALTERA
5SGXMA5N2F45I4N	132	BGA	20+	ALTERA
5SGXMA7K2F40C2N	168	BGA	20+	ALTERA
5SGXMA7K3F40C2N	168	FBGA1156	20+	ALTERA
5SGXMA9K3H40C2N	103	BGA	20+	ALTERA
5SGXMA9K3H40I3N	156	BGA	20+	ALTERA
5SGXMA9K3H40I4N	142	BGA	20+	ALTERA
EP1S20F484C6	1000	BGA	20+	XILINX
EP1S20F484C6N	1000	BGA	20+	XILINX
EP1S20F484I6	100	BGA	20+	ALTERA
EP1S20F484I6N	187	BGA484	20+	ALTERA
EP1S20F672I7	1500	BGA	20+	ALTERA
EP1S20F672I7N	150	FBGA676	20+	ALTERA
EP1S20F780I6	72	BGA	20+	ALTERA
EP1S25F1020C6	300	FCBGA	20+	ALTERA
EP1S25F1020I6	38	BGA	20+	ALTERA
EP1S25F1020I6N	120	FBGA	20+	ALTERA
EP1S25F672C6	144	BGA	20+	ALTERA
EP1S25F672C6N	160	FCBGA	20+	ALTERA
EP1S25F672C7	500	BGA	20+	ALTERA
EP1S25F672C7N	200	FBGA	20+	ALTERA
EP1S25F672I7	500	BGA	20+	ALTERA
EP1S25F780C7N	248	BGA1136	20+	ALTERA
EP1S25F780I6	42	BGA	20+	ALTERA
EP1S30F1020I6	168	BGA	20+	ALTERA
EP1S30F1020I6N	50	BGA	20+	ALTERA
EP1S30F780I6	172	BGA	20+	ALTERA
EP1S30F780I6N	195	FBGA676	20+	ALTERA
EP1S40B956I6	228	BGA	20+	ALTERA
EP1S40F1020I6	480	BGA	20+	ALTERA

EP2AGX190EF29C5N	117	BGA	20+	ALTERA
EP2AGX190EF29C6G	172	BGA	20+	XILINX
EP2AGX190EF29C6N	461	BGA	20+	ALTERA
EP2AGX190EF29I3N	96	BGA	20+	ALTERA
EP2AGX190EF29I5N	55	BGA	20+	Intel/Altera
EP2AGX190FF35C5N	500	BGA	20+	ALTERA
EP2AGX190FF35C6N	30	BGA	20+	ALTERA
EP2AGX190FF35I3N	400	FBGA665	20+	ALTERA
EP2AGX190FF35I5N	1080	TQFP	20+	ALTERA
EP2AGX260EF29C5N	12	BGA	20+	ALTERA
EP2AGX260EF29C6N	25	BGA	20+	Intel/Altera
EP2AGX260EF29I3N	25	BGA	20+	Intel/Altera
EP2AGX260FF35C4N	2000	SOP	20+	ALTERA
EP2AGX260FF35C6N	110	FBGA	20+	ALTERA
EP2AGX260FF35I3N	263	FCBGA676	20+	ALTERA
EP2AGX260FF35I5N	165	BGA	20+	ALTERA
EP2AGX45CU17C4N	50	BGA	20+	ALTERA
EP2AGX45CU17I3G	50	BGA	20+	ALTERA
EP2AGX45DF25I3N	100	FBGA1156	20+	ALTERA
EP2AGX45DF29C5N	293	FCBGA1152	20+	ALTERA
EP2AGX45DF29I3N	167	FBGA1156	20+	ALTERA
EP2AGX65DF25C6N	263	FCBGA1738	20+	ALTERA
EP2AGX65DF25I3N	500	BGA900	20+	ALTERA
EP2AGX65DF25I5N	190	BGA2397	20+	XILINX
EP2AGX65DF25I5N	120	FBGA	20+	ALTERA
EP2AGX65DF29C4N	120	FBGA	20+	ALTERA
EP2AGX65DF29C5N	45	BGA	20+	ALTERA
EP2AGX65DF29C6N	116	FCBGA1517	20+	ALTERA
EP2AGX65DF29I3N	60	BGA	20+	Intel/Altera
EP2AGX65DF29I3N	133	FCBGA1517	20+	ALTERA
EP2AGX65DF29I5N	172	BGA	20+	ALTERA
EP2AGX95DF25C4N	200	FCBGA	20+	ALTERA
EP2AGX95DF25C6N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I5N	58	FPBGA1020	20+	ALTERA
EP2AGX95EF29C4N	1080	BGA	20+	ALTERA

Figure 2–51. M4K RAM Block Control Signals



The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–52 shows the M4K RAM block to logic array interface.