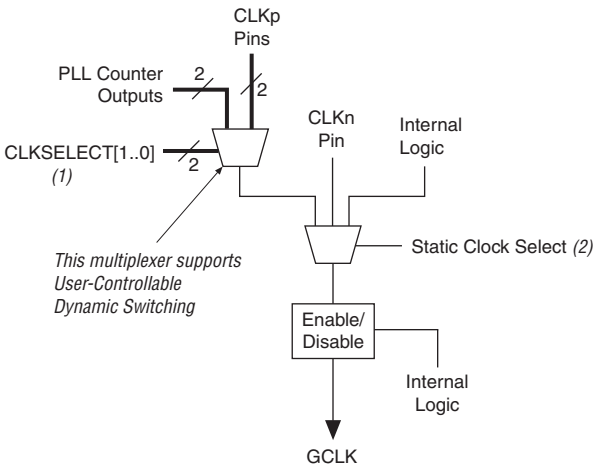
When using the global or regional clock control blocks in Stratix II devices to select between multiple clocks or to enable and disable clock networks, be aware of possible narrow pulses or glitches when switching from one clock signal to another. A glitch or runt pulse has a width that is less than the width of the highest frequency input clock signal. To prevent logic errors within the FPGA, Altera recommends that you build circuits that filter out glitches and runt pulses.

Figures 2–37 through 2–39 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

***Figure 2–37. Global Clock Control Blocks***




***Notes to Figure 2–37:***

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

芯片详细信息

| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>EP2S130F780I4N | Rohs Code:<br>Yes | Part Life Cycle Code:<br>Active | Ihs Manufacturer:<br>INTEL CORP |
| Package Description:<br>29 X 29 MM, 1 MM PITCH, LEAD FREE, FBGA-780 | Reach Compliance Code:<br>compliant | ECCN Code:<br>3A001.A.7.A | HTS Code:<br>8542.39.00.01 |
| Manufacturer:<br>Intel Corporation | Risk Rank:<br>5.26 | Clock Frequency-Max:<br>717 MHz | Combinatorial Delay of a CLB-Max:<br>5.117 ns |
| JESD-30 Code:<br>S-PBGA-B780 | JESD-609 Code:<br>e1 | Length:<br>29 mm | Moisture Sensitivity Level:<br>3 |
| Number of CLBs:<br>6627 | Number of Inputs:<br>534 | Number of Logic Cells:<br>132540 | Number of Outputs:<br>526 |
| Number of Terminals:<br>780 | Operating Temperature-Max:<br>100 °C | Operating Temperature-Min:<br>-40 °C | Organization:<br>6627 CLBS |
| Package Body Material:<br>PLASTIC/EPOXY | Package Code:<br>BGA | Package Equivalence Code:<br>BGA780,28X28,40 | Package Shape:<br>SQUARE |
| Package Style:<br>GRID ARRAY | Peak Reflow Temperature (Cel):<br>245 | Power Supplies:<br>1.2,1.5/3.3,3.3 V | Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY |
| Qualification Status:<br>Not Qualified | Seated Height-Max:<br>3.5 mm | Subcategory:<br>Field Programmable Gate Arrays | Supply Voltage-Max:<br>1.25 V |
| Supply Voltage-Min:<br>1.15 V | Supply Voltage-Nom:<br>1.2 V | Surface Mount:<br>YES | Technology:<br>CMOS |
| Temperature Grade:<br>INDUSTRIAL | Terminal Finish:<br>TIN SILVER COPPER | Terminal Form:<br>BALL | Terminal Pitch:<br>1 mm |
| Terminal Position:<br>BOTTOM | Time@Peak Reflow Temperature-Max (s):<br>40 | Width:<br>29 mm | |

| | | |
|---|---|---|
| RoHS: | RoHS 详细信息 | |
| 产品: | Stratix II | ☐ |
| 系列: | Stratix II EP2S130 | ☐ |
| 逻辑元件数量: | 132540 LE | ☐ |
| 自适应逻辑模块 - ALM: | 53016 ALM | ☐ |
| 嵌入式内存: | 6.44 Mbit | ☐ |
| 输入/输出端数量: | 534 I/O | ☐ |
| 工作电源电压: | 1.2 V | ☐ |
| 最小工作温度: | - 40 C | ☐ |
| 最大工作温度: | + 85 C | ☐ |
| 安装风格: | SMD/SMT | ☐ |
| 封装 / 箱体: | FBGA-780 | ☐ |
| 封装: | Tray | ☐ |
| 商标: | Intel / Altera | |
| 湿度敏感性: | Yes | |
| 逻辑数组块数量——LAB: | 6627 LAB | |
| 工作电源电流: | 820 mA | |
| 产品类型: | FPGA - Field Programmable Gate Array | |
| 工厂包装数量: | 36 | |
| 子类别: | Programmable Logic ICs | |
| 总内存: | 6747840 bit | |
| 商标名: | Stratix II | |
| 零件号别名: | 974298 | |

*Table 3–1. Stratix II JTAG Instructions*

| JTAG Instruction | Instruction Code | Description |
|---|---|---|
| SAMPLE/PRELOAD | 00 0000 0101 | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer. |
| EXTEST *(1)* | 00 0000 1111 | Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | 11 1111 1111 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | 00 0000 0111 | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | 00 0000 0110 | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| HIGHZ *(1)* | 00 0000 1011 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |
| CLAMP *(1)* | 00 0000 1010 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | | Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner. |
| PULSE_NCONFIG | 00 0000 0001 | Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected. |
| CONFIG_IO *(2)* | 00 0000 1101 | Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state. |
| SignalTap II instructions | | Monitors internal device operation with the SignalTap II embedded logic analyzer. |

***Notes to Table 3–1:***

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. Turn on the **Auto Usercode** option by clicking **Device & Pin Options**, then **General,** in the **Settings** dialog box (Assignments menu).

*Table 3–2. Stratix II Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP2S15 | 1,140 |
| EP2S30 | 1,692 |
| EP2S60 | 2,196 |
| EP2S90 | 2,748 |
| EP2S130 | 3,420 |
| EP2S180 | 3,948 |

*Table 3–3. 32-Bit Stratix II Device IDCODE*

| Device | IDCODE (32 Bits) *(1)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) *(2)* |
| EP2S15 | 0000 | 0010 0000 1001 0001 | 000 0110 1110 | 1 |
| EP2S30 | 0000 | 0010 0000 1001 0010 | 000 0110 1110 | 1 |
| EP2S60 | 0001 | 0010 0000 1001 0011 | 000 0110 1110 | 1 |
| EP2S90 | 0000 | 0010 0000 1001 0100 | 000 0110 1110 | 1 |
| EP2S130 | 0000 | 0010 0000 1001 0101 | 000 0110 1110 | 1 |
| EP2S180 | 0000 | 0010 0000 1001 0110 | 000 0110 1110 | 1 |

*Notes to Table 3–3:*
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Stratix, Stratix II, Cyclone, and Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix, Stratix II, Cyclone, and Cyclone II devices are in the 18th or after they fail configuration. This does not affect SignalTap II.