1. Stratix III Device Data Sheet: DC and Switching Characteristics

SIII52001-2.1

Electrical Characteristics

Operating Conditions

When Stratix® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix III devices, system designers must consider the operating requirements discussed in this chapter. Stratix III devices are offered in both commercial and industrial grades. Commercial devices are offered in –2 (fastest), –3, –4 and –4L speed grades. Industrial devices are offered only in –3, –4, and –4L speed grades.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with "C" prefix and industrial with "I" prefix. Commercial devices are therefore indicated as C2, C3, C4, and C4L per respective speed grades. Industrial devices are indicated as I3, I4, and I4L.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods may have adverse effects on the device.

Table 1–1. Stratix III Device Absolute Maximum Ratings *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
V_{CCL}	Selectable core voltage power supply	-0.5	1.65	V
V_{CC}	I/O registers power supply	-0.5	1.65	V
V_{CCD_PLL}	PLL digital power supply	-0.5	1.65	V
V_{CCA_PLL}	PLL analog power supply	-0.5	3.75	V
V_{CCPT}	Programmable power technology power supply	-0.5	3.75	V
V_{CCPGM}	Configuration pins power supply	-0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V_{CCIO}	I/O power supply	-0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply (top and bottom I/O banks only)	-0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_I	DC Input voltage	-0.5	4.0	V

Table 1–8. Stratix III On-Chip Termination Resistance Tolerance Specification

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3, I3	C4, I4	
R_{OCT_UNCAL}	Internal series termination without calibration	—				
25-Ω R_S 3.3/3.0/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/3.0/2.5 V	±30	±40	±40	%
25-Ω R_S 1.8/1.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8/1.5 V	±30	±50	±50	%
25-Ω R_S 1.2	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±35	±60	±60	%
50-Ω R_S 3.3/3.0/2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/3.0/2.5 V	±30	±40	±40	%
50-Ω R_S 1.8/1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8/1.5 V	±30	±50	±50	%
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±35	±60	±60	%

Table 1–9 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–9 and Equation 1–1 to determine OCT variation without re-calibration.

Equation 1–1. OCT Variation Without Re-Calibration *(Note 1)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

Notes to Equation 1–1:

(1) R_{OCT} value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1–9. On-Chip Termination Variation after Power-up Calibration (Part 1 of 2) *(Note 1)*

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3	0.029	%/mV
		2.5	0.036	%/mV
		1.8	0.065	%/mV
		1.5	0.104	%/mV
		1.2	0.177	%/mV

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Stratix II	☐
系列:	Stratix II EP2S15	☐
逻辑元件数量:	15600 LE	☐
自适应逻辑模块 - ALM:	6240 ALM	☐
嵌入式内存:	409.5 kbit	☐
输入/输出端数量:	366 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-672	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	780 LAB	
工作电源电流:	250 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	40	
子类别:	Programmable Logic ICs	
总内存:	419328 bit	
商标名:	Stratix II	
零件号别名:	967195	

Table 1–79. EP3SL150 Column Pins output Timing Parameters (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.132	3.370	4.770	5.169	5.682	5.543	5.827	5.292	5.804	5.668	5.901	ns
		GCLK PLL	t_{co}	1.340	1.520	1.968	2.068	2.284	2.295	2.322	2.173	2.391	2.401	2.309	ns
	6mA	GCLK	t_{co}	3.118	3.356	4.758	5.158	5.672	5.533	5.817	5.282	5.795	5.659	5.892	ns
		GCLK PLL	t_{co}	1.326	1.506	1.956	2.057	2.274	2.285	2.312	2.163	2.382	2.392	2.300	ns
	8mA	GCLK	t_{co}	3.106	3.343	4.741	5.140	5.654	5.515	5.799	5.264	5.777	5.641	5.874	ns
		GCLK PLL	t_{co}	1.314	1.493	1.939	2.039	2.256	2.267	2.294	2.145	2.364	2.374	2.282	ns
	10mA	GCLK	t_{co}	3.106	3.343	4.744	5.144	5.658	5.519	5.803	5.268	5.782	5.646	5.879	ns
		GCLK PLL	t_{co}	1.314	1.493	1.942	2.043	2.260	2.271	2.298	2.149	2.369	2.379	2.287	ns
	12mA	GCLK	t_{co}	3.102	3.339	4.737	5.136	5.651	5.512	5.796	5.261	5.774	5.638	5.871	ns
		GCLK PLL	t_{co}	1.310	1.489	1.935	2.035	2.253	2.264	2.291	2.142	2.361	2.371	2.279	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{co}	3.106	3.341	4.730	5.127	5.639	5.500	5.784	5.250	5.761	5.625	5.858	ns
		GCLK PLL	t_{co}	1.314	1.491	1.928	2.026	2.241	2.252	2.279	2.131	2.348	2.358	2.266	ns
	16mA	GCLK	t_{co}	3.107	3.343	4.738	5.137	5.650	5.511	5.795	5.260	5.773	5.637	5.870	ns
		GCLK PLL	t_{co}	1.315	1.493	1.936	2.036	2.252	2.263	2.290	2.141	2.360	2.370	2.278	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{co}	3.135	3.373	4.769	5.167	5.680	5.541	5.825	5.291	5.802	5.666	5.899	ns
		GCLK PLL	t_{co}	1.343	1.523	1.967	2.066	2.282	2.293	2.320	2.172	2.389	2.399	2.307	ns
	6mA	GCLK	t_{co}	3.124	3.361	4.757	5.155	5.668	5.529	5.813	5.279	5.790	5.654	5.887	ns
		GCLK PLL	t_{co}	1.332	1.511	1.955	2.054	2.270	2.281	2.308	2.160	2.377	2.387	2.295	ns
	8mA	GCLK	t_{co}	3.119	3.357	4.757	5.156	5.669	5.530	5.814	5.280	5.792	5.656	5.889	ns
		GCLK PLL	t_{co}	1.327	1.507	1.955	2.055	2.271	2.282	2.309	2.161	2.379	2.389	2.297	ns
	10mA	GCLK	t_{co}	3.105	3.342	4.739	5.137	5.650	5.511	5.795	5.261	5.774	5.638	5.871	ns
		GCLK PLL	t_{co}	1.313	1.492	1.937	2.036	2.252	2.263	2.290	2.142	2.361	2.371	2.279	ns
	12mA	GCLK	t_{co}	3.103	3.340	4.737	5.135	5.648	5.509	5.793	5.259	5.771	5.635	5.868	ns
		GCLK PLL	t_{co}	1.311	1.490	1.935	2.034	2.250	2.261	2.288	2.140	2.358	2.368	2.276	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{co}	3.107	3.342	4.729	5.125	5.636	5.497	5.781	5.248	5.758	5.622	5.855	ns
		GCLK PLL	t_{co}	1.315	1.492	1.927	2.024	2.238	2.249	2.276	2.129	2.345	2.355	2.263	ns
	16mA	GCLK	t_{co}	3.107	3.343	4.737	5.135	5.648	5.509	5.793	5.259	5.771	5.635	5.868	ns
		GCLK PLL	t_{co}	1.315	1.493	1.935	2.034	2.250	2.261	2.288	2.140	2.358	2.368	2.276	ns

芯片详细信息

Manufacturer Part Number: EP2S15F672C5N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: 35 X 35 MM, 1 MM PITCH, FBGA-672	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.29	Clock Frequency-Max: 640 MHz	Combinatorial Delay of a CLB-Max: 5.962 ns
JESD-30 Code: S-PBGA-B672	JESD-609 Code: e1	Length: 35 mm	Moisture Sensitivity Level: 3
Number of CLBs: 6240	Number of Inputs: 366	Number of Logic Cells: 15600	Number of Outputs: 358
Number of Terminals: 672	Operating Temperature-Max: 85 °C	Organization: 6240 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA672,26X26,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 245	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2.6 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: Tin/Silver/Copper (Sn/Ag/Cu)	Terminal Form: BALL	Terminal Pitch: 1.27 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 40	Width: 35 mm		