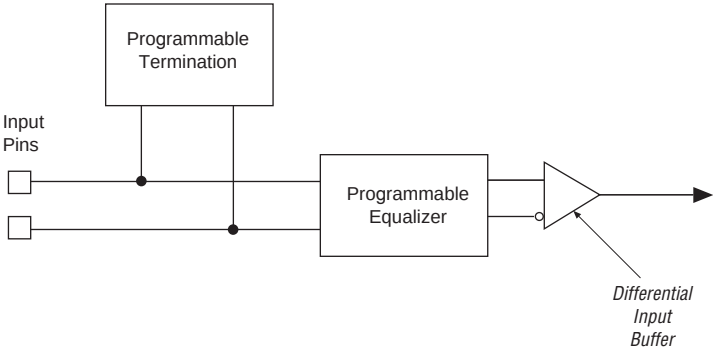
- Lane deskew
- Rate matcher
- 8B/10B decoder
- Byte deserializer
- Byte ordering
- Receiver phase compensation FIFO buffer

### *Receiver Input Buffer*

The Stratix II GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and the 1.2 V common mode voltage for DC-coupled LVDS links.

The receiver has programmable on-chip 100-, 120-, or 150-Ω differential termination for different protocols, as shown in Figure 2–12. The receiver's internal termination can be disabled if external terminations and biasing are provided. The receiver and transmitter differential termination resistances can be set independently of each other.

***Figure 2–12. Receiver Input Buffer***




### *Programmable Termination*

The programmable termination can be statically set in the Quartus II software. Figure 2–13 shows the setup for programmable receiver termination. The termination can be disabled if external termination is provided.

# PLLs and Clock Networks

Stratix II GX devices provide a hierarchical clock structure and multiple phase-locked loops (PLLs) with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

## Global and Hierarchical Clocking

Stratix II GX devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II GX devices.

There are 12 dedicated clock pins to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–61 and 2–62. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. Table 2–24 shows global and regional clock features.

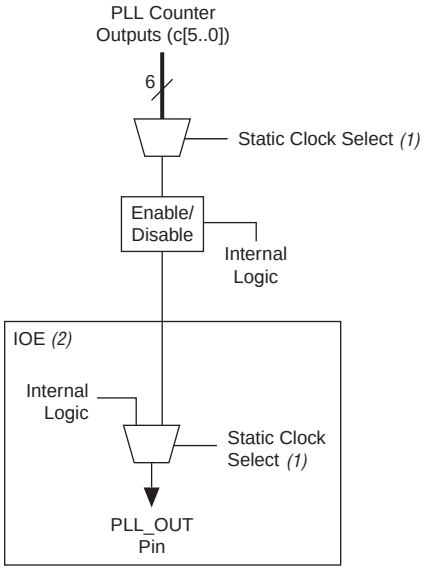
*Table 2–24. Global and Regional Clock Features*

| Feature | Global Clocks | Regional Clocks |
|---|---|---|
| Number per device | 16 | 32 |
| Number available per quadrant | 16 | 8 |
| Sources | Clock pins, PLL outputs, core routings, inter-transceiver clocks | Clock pins, PLL outputs, core routings, inter-transceiver clocks |
| Dynamic clock source selection | ✓ | — |
| Dynamic enable/disable | ✓ | ✓ |

### *Global Clock Network*

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally

*Figure 2–69. External PLL Output Clock Control Blocks*




*Notes to Figure 2–69:*

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or you can control the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

芯片详细信息

| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>EP2S15F672C3 | Rohs Code:<br>No | Part Life Cycle Code:<br>Not Recommended | Ihs Manufacturer:<br>INTEL CORP |
| Package Description:<br>35 X 35 MM, 1 MM PITCH, FBGA-672 | Reach Compliance Code:<br>compliant | ECCN Code:<br>3A991 | HTS Code:<br>8542.39.00.01 |
| Manufacturer:<br>Intel Corporation | Risk Rank:<br>5.29 | Clock Frequency-Max:<br>717 MHz | Combinatorial Delay of a CLB-Max:<br>4.45 ns |
| JESD-30 Code:<br>S-PBGA-B672 | JESD-609 Code:<br>e0 | Length:<br>35 mm | Moisture Sensitivity Level:<br>3 |
| Number of CLBs:<br>6240 | Number of Inputs:<br>366 | Number of Logic Cells:<br>15600 | Number of Outputs:<br>358 |
| Number of Terminals:<br>672 | Operating Temperature-Max:<br>85 °C | Organization:<br>6240 CLBS | Package Body Material:<br>PLASTIC/EPOXY |
| Package Code:<br>BGA | Package Equivalence Code:<br>BGA672,26X26,40 | Package Shape:<br>SQUARE | Package Style:<br>GRID ARRAY |
| Peak Reflow Temperature (Cel):<br>220 | Power Supplies:<br>1.2,1.5/3.3,3.3 V | Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY | Qualification Status:<br>Not Qualified |
| Seated Height-Max:<br>2.6 mm | Subcategory:<br>Field Programmable Gate Arrays | Supply Voltage-Max:<br>1.25 V | Supply Voltage-Min:<br>1.15 V |
| Supply Voltage-Nom:<br>1.2 V | Surface Mount:<br>YES | Technology:<br>CMOS | Temperature Grade:<br>OTHER |
| Terminal Finish:<br>TIN LEAD | Terminal Form:<br>BALL | Terminal Pitch:<br>1.27 mm | Terminal Position:<br>BOTTOM |
| Time@Peak Reflow Temperature-Max (s):<br>30 | Width:<br>35 mm | | |

| | | |
|---|---|---|
| 产品种类: | FPGA - 现场可编程门阵列 | ☑ |
| RoHS: | N | |
| 产品: | Stratix II | ☐ |
| 系列: | Stratix II EP2S15 | ☐ |
| 逻辑元件数量: | 15600 LE | ☐ |
| 自适应逻辑模块 - ALM: | 6240 ALM | ☐ |
| 嵌入式内存: | 409.5 kbit | ☐ |
| 输入/输出端数量: | 366 I/O | ☐ |
| 工作电源电压: | 1.2 V | ☐ |
| 最小工作温度: | 0 C | ☐ |
| 最大工作温度: | + 70 C | ☐ |
| 安装风格: | SMD/SMT | ☐ |
| 封装 / 箱体: | FBGA-672 | ☐ |
| 封装: | Tray | ☐ |
| 商标: | Intel / Altera | |
| 湿度敏感性: | Yes | |
| 逻辑数组块数量——LAB: | 780 LAB | |
| 工作电源电流: | 250 mA | |
| 产品类型: | FPGA - Field Programmable Gate Array | |
| 工厂包装数量: | 40 | |
| 子类别: | Programmable Logic ICs | |
| 总内存: | 419328 bit | |
| 商标名: | Stratix II | |
| 零件号别名: | 966853 | |