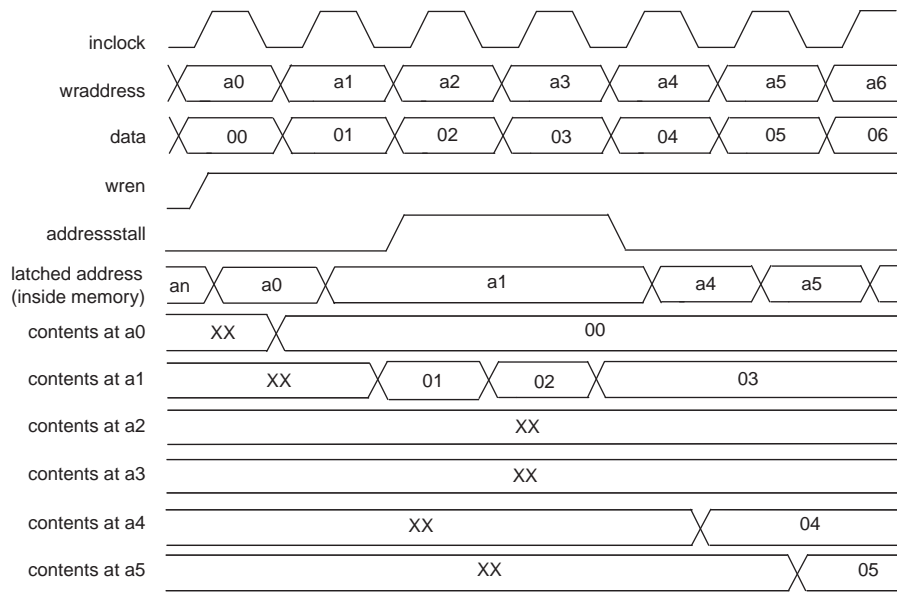Figure 4–6 shows the address clock enable waveform during the write cycle for MLABs.

Figure 4–6. Stratix III Address Clock Enable during Write Cycle Waveform for MLABs


Mixed Width Support

M9K and M144K memory blocks inherently support mixed data widths. MLABs can support mixed data widths through emulation via the Quartus II software. When using simple dual-port or true dual-port mixed width support allows you to read and write different data widths to a memory block. Refer to "Memory Modes" on page 4–10 for details on the different widths supported per memory mode.

☞ You cannot use the ECC on M144 memory blocks when using the mixed width support.

☞ MLABs do not support mixed-width FIFO mode.

Asynchronous Clear

Stratix III M9K and M144K memory blocks support asynchronous clears on the output latches and output registers. MLABs supports asynchronous clear on the output registers only as the output is not latched. Therefore, if your M9K and M144K are not using the output registers, you can still clear the RAM outputs via the output latch asynchronous clear. The functional waveform in Figure 4–7 shows this functionality.

Figure 4–7. Output Latch Asynchronous Clear Waveform
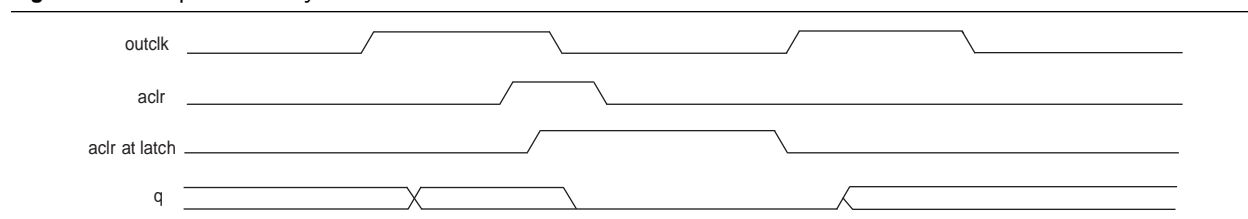
You can selectively enable asynchronous clears per logical memory via the Quartus II RAM MegaWizard Plug-In Manager.

For more information, refer to the *RAM Megafunction User Guide*.

Error Correction Code Support

Stratix III M144K blocks have built-in support for error correction code (ECC) when in ×64-wide simple dual-port mode. ECC allows you to detect and correct data errors in the memory array. The M144K blocks have a single-error-correction double-error-detection (SECDED) implementation. SECDED can detect and fix a single-bit error in a 64-bit word or detect two-bit errors in a 64-bit word. It cannot detect three or more errors.

The M144K ECC status is communicated via a three-bit status flag `eccstatus[2..0]`. The status flag can be either registered or unregistered. When registered, it uses the same clock and asynchronous clear signals as the output registers. When not registered, it cannot be asynchronously cleared.

Table 4–3 shows the truth table for the ECC status flags.

Table 4–3. Truth Table for ECC Status Flags

Status	eccstatus[2]	eccstatus[1]	eccstatus[0]
No error	0	0	0
Single error and fixed	0	1	1
Double error and no fix	1	0	1
Illegal	0	0	1
Illegal	0	1	0
Illegal	1	0	0
Illegal	1	1	X

You cannot use the byte-enable feature when ECC is engaged.

Read during write "old data" mode is not supported when ECC is engaged.

EP2S60F672C3	10	BGA	20+	ALTERA
EP2S60F672C3N	115	BGA	20+	ALTERA
EP2S60F672C3N	105	FCBGA	20+	ALTERA
EP2S60F672C4	200	FCBGA	20+	ALTERA
EP2S60F672C4N	200	FCBGA	20+	ALTERA
EP2S60F672C5	160	FCBGA	20+	ALTERA
EP2S60F672C5N	3447	BGA	20+	ALTERA
EP2S60F672I4	160	FCBGA	20+	ALTERA
EP2S60F672I4N	911	BGA	20+	ALTERA
EP2S60F672I4N	347	FCBGA668	20+	ALTERA
EP2S60F672I5	3000	BGA	20+	ALTERA
EP2S60F672I5N	116	FBGA676	20+	ALTERA
EP2S90F1020C3	122	BGA	20+	ALTERA
EP2S90F1020C3N	120	FBGA	20+	ALTERA
EP2S90F1020C4	120	FBGA	20+	ALTERA
EP2S90F1020C4N	300	FBGA	20+	ALTERA
EP2S90F1020C4N	300	BGA	20+	ALTERA
EP2S90F1020C5N	368	FCBGA1156	20+	ALTERA
EP2S90F1020I3N	482	BGA	20+	ALTERA
EP2S90F1020I4N	897	BGA	20+	ALTERA
EP2S90F1020I4N	50	BGA	20+	ALTERA/INTER
EP2S90F1020I4N	283	FCBGA901	20+	ALTERA
EP2S90F1508C5N	448	BGA	20+	ALTERA
EP2SGX130GF1508C3N	6	BGA	20+	Intel/Altera
EP2SGX130GF1508C3N	109	FCBGA900	20+	ALTERA
EP2SGX130GF1508C4N	80	BGA	20+	ALTERA
EP2SGX130GF1508C5N	488	BGA	20+	ALTERA
EP2SGX130GF1508I4N	47	BGA	20+	Intel/Altera
EP2SGX130GF1508I4N	280	BGA	20+	ALTERA
EP2SGX30DF780I4N	63	FBGA1761	20+	ALTERA
EP2SGX60CF780I4	69	BGA	20+	ALTERA
EP2SGX60EF1152C3N	163	BGA	20+	ALTERA
EP2SGX60EF1152C3N	50	BGA	20+	Intel/Altera
EP2SGX60EF1152C4N	120	BGA	20+	ALTERA
EP2SGX60EF1152C4N	57	BGA	20+	Intel/Altera
EP2SGX60EF1152C5N	200	BGA	20+	ALTERA
EP2SGX60EF1152I3N	120	BGA	20+	ALTERA

Figure 6–44. Dynamic Phase Shifting Waveform
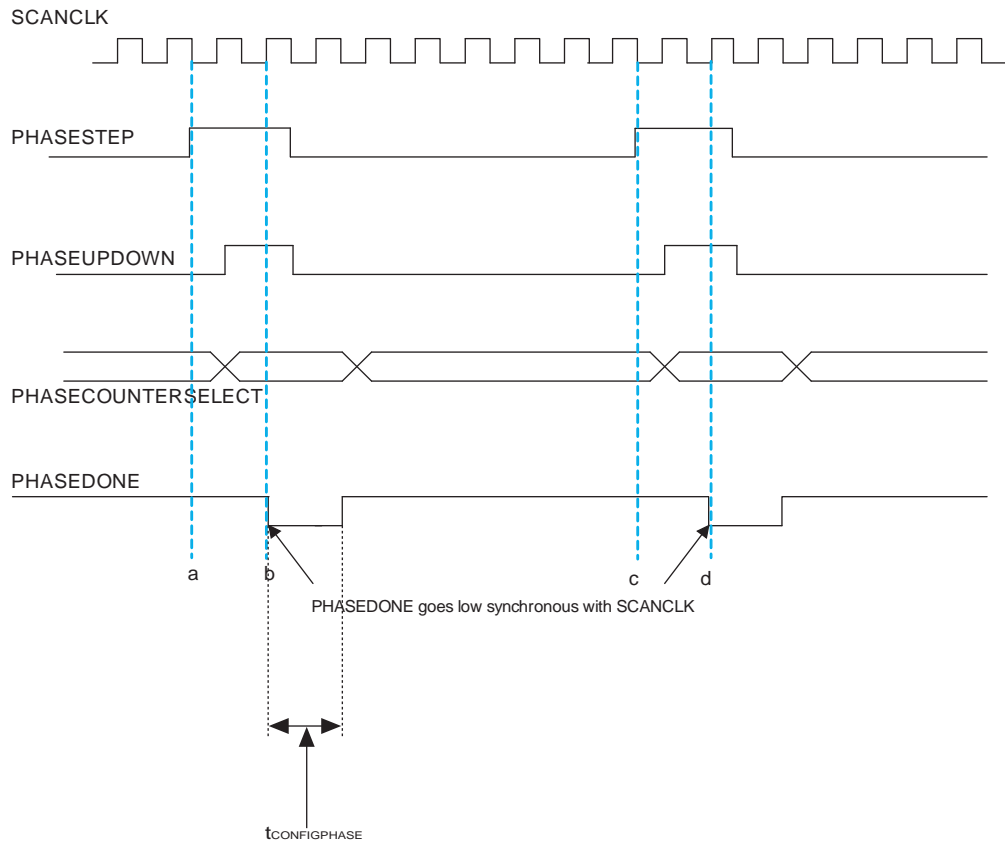
Dynamic phase-shifting can be repeated indefinitely. All signals are synchronous to scanclk and must meet t_{su}/t_h requirements with respect to scanclk edges.

The phasestep signal is latched on the negative edge of scanclk. In Figure 6–44, this is shown by the second scanclk falling edge. phasestep must stay high for at least two scanclk cycles. On the second scanclk rising edge after phasestep is latched (the fourth scanclk rising edge in Figure 6–44), the values of phaseupdown and phasecounterselect are latched and the PLL starts dynamic phase-shifting for the specified counters and in the indicated direction. On the fourth scanclk rising edge, phasedone goes high to low and remains low until the PLL finishes dynamic phase-shifting. You can perform another dynamic phase-shift after the phasedone signal goes from low to high.

Depending on the VCO and scanclk frequencies, phasedone low time ($t_{CONFIGPHASE}$) may be greater than or less than one scanclk cycle.

After phasedone goes from low to high, you can perform another dynamic phase shift. Phasestep pulses must be at least one scanclk cycle apart.

For more information about the ALTPLL_RECONFIG MegaWizard Plug-In Manager, refer to the *ALTPLL_RECONFIG Megafunction User Guide*.

EP2SGX90EF1152I4N	16	BGA	20+	Intel/Altera
EP2SGX90EF1152I4N	98	FCBGA1158	20+	ALTERA
EP2SGX90FF1508C3N	10	BGA	20+	ALTERA
EP3SE110F1152C2N	88	BGA	20+	ALTERA
EP3SE110F1152C4N	100	BGA	20+	ALTERA
EP3SE110F1152I3N	1036	BGA	20+	ALTERA
EP3SE110F1152I3N	125	FCBGA1158	20+	ALTERA
EP3SE110F1152I4N	65	BGA	20+	ALTERA
EP3SE110F1152I4N	3	BGA	20+	Intel/Altera
EP3SE110F780I3N	4	BGA	20+	Intel/Altera
EP3SE110F780I3N	140	CFP	20+	ALTERA
EP3SE110F780I4N	280	BGA	20+	ALTERA
EP3SE260F1152C2N	143	BGA	20+	ALTERA
EP3SE260F1152C4N	56	BGA	20+	ALTERA
EP3SE260F1152I3N	103	FCBGA1517	20+	ALTERA
EP3SE260F1152I4N	11335	SOT-23	20+	ALTERA
EP3SE260F1517C4N	120	BGA	20+	ALTERA
EP3SE260H780C4N	168	BGA	20+	ALTERA
EP3SE50F780C2N	473	BGA	20+	ALTERA
EP3SE50F780C3N	50	BGA	20+	ALTERA
EP3SE50F780C4N	10	BGA	20+	ALTERA
EP3SE50F780I3N	368	FCBGA1148	20+	ALTERA
EP3SE50F780I4N	178	FCBGA665	20+	ALTERA
EP3SE80F1152I3N	2	BGA	20+	Intel/Altera
EP3SE80F1152I4N	136	BGA	20+	ALTERA
EP3SE80F1152I4N	3	BGA	20+	Intel/Altera
EP3SE80F780C3N	466	BGA	20+	ALTERA
EP3SE80F780I3N	151	BGA	20+	ALTERA
EP3SL110F1152C2N	100	BGA	20+	ALTERA
EP3SL110F1152I3N	166	FCBGA1759	20+	ALTERA
EP3SL110F780C2N	168	FCBGA2104	20+	ALTERA
EP3SL110F780C3N	57	BGA	20+	Intel/Altera
EP3SL110F780C4N	156	BGA	20+	ALTERA
EP3SL110F780I3LN	50	BGA	20+	ALTERA
EP3SL110F780I3N	120	BGA	20+	ALTERA
EP3SL110F780I4LN	25	BGA	20+	ALTERA
EP3SL110F780I4N	6	BGA	20+	Intel/Altera