PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (`CLK[15..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	`CLK` pins, PLL outputs, or internal logic	`CLK` pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

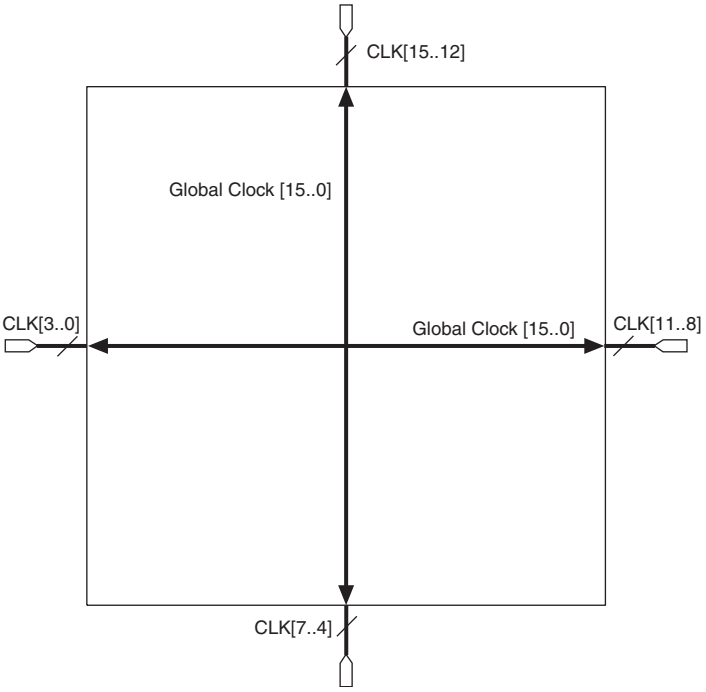
Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between `CLKp` pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–31 shows the 16 dedicated CLK pins driving global clock networks.

Figure 2–31. Global Clocking



Regional Clock Network

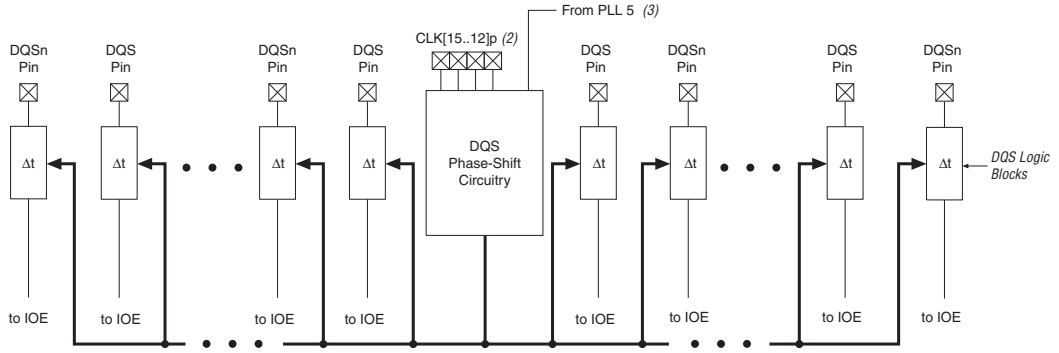
There are eight regional clock networks RCLK[7..0] in each quadrant of the Stratix II device that are driven by the dedicated CLK[15..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK clock pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–32.

芯片详细信息

Manufacturer Part Number: EP2S15F484I5	Rohs Code: No	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Reach Compliance Code: compliant	Manufacturer: Intel Corporation	Risk Rank: 5.59	JESD-30 Code: S-PBGA-B484
JESD-609 Code: e0	Moisture Sensitivity Level: 3	Number of Inputs: 342	Number of Logic Cells: 15600
Number of Outputs: 334	Number of Terminals: 484	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA484,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Power Supplies: 1.2,1.5/3.3,3.3 V
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Subcategory: Field Programmable Gate Arrays	Surface Mount: YES
Technology: CMOS	Terminal Finish: Tin/Lead (Sn/Pb)	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM			

EP3SE50F780I3N	368	FCBGA1148	20+	ALTERA
EP3SE50F780I4N	178	FCBGA665	20+	ALTERA
EP3SE80F1152I3N	2	BGA	20+	Intel/Altera
EP3SE80F1152I4N	136	BGA	20+	ALTERA
EP3SE80F1152I4N	3	BGA	20+	Intel/Altera
EP3SE80F780C3N	466	BGA	20+	ALTERA
EP3SE80F780I3N	151	BGA	20+	ALTERA
EP3SL110F1152C2N	100	BGA	20+	ALTERA
EP3SL110F1152I3N	166	FCBGA1759	20+	ALTERA
EP3SL110F780C2N	168	FCBGA2104	20+	ALTERA
EP3SL110F780C3N	57	BGA	20+	Intel/Altera
EP3SL110F780C4N	156	BGA	20+	ALTERA
EP3SL110F780I3LN	50	BGA	20+	ALTERA
EP3SL110F780I3N	120	BGA	20+	ALTERA
EP3SL110F780I4LN	25	BGA	20+	ALTERA
EP3SL110F780I4N	6	BGA	20+	Intel/Altera
EP3SL110F780I4N	280	BGA	20+	ALTERA
EP3SL150F1152C4N	5	BGA	20+	Intel/Altera
EP3SL150F1152C4N	163	FBGA900	20+	ALTERA
EP3SL150F1152C4N	1000	BGA	20+	ALTERA
EP3SL150F1152I3N	300	BGA	20+	ALTERA
EP3SL150F1152I4N	500	BGA	20+	ALTERA
EP3SL150F780C2N	152	BGA	20+	ALTERA
EP3SL150F780I3N	1010	SOP	20+	ALTERA
EP3SL200F1152I3N	228	BGA	20+	ALTERA
EP3SL200F1152I4N	105	FBGA676	20+	ALTERA
EP3SL200F1517C3N	70	BGA	20+	ALTERA
EP3SL200H28I3N	50	BGA	20+	XILINX
EP3SL200H780C4N	285	FBGA780	20+	ALTERA
EP3SL260F1517C3N	68	BGA	20+	ALTERA
EP3SL340F1517C2N	200	BGA	20+	ALTERA
EP3SL340F1517C3N	100	BGA	20+	ALTERA
EP3SL340F1517C4N	105	BGA	20+	ALTERA
EP3SL340F1517I3N	3	BGA	20+	Intel/Altera
EP3SL340F1517I3N	371	FCBGA1136	20+	ALTERA
EP3SL340F1517I4N	321	BGA	20+	ALTERA
EP3SL340H1152I3N	136	BGA	20+	Intel/Altera

Figure 2–56. DQS Phase-Shift Circuitry Notes (1), (2), (3), (4)



Notes to Figure 2–56:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The Δt module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phase-shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.