Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfacing, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. For example, Stratix III devices I/O configured with voltage referenced I/O standards can achieve up to the stated system interfacing speed as indicated in "External Memory Interface Specifications" on page 1–25. General-purpose I/O standards such as 3.3, 3.0, 2.5, 1.8, or 1.5 LVTTL/LVCMOS are capable of typical 167 MHz and 1.2 LVCMOS at 100MHz interfacing frequency with 10pF load.

☞ Actual achievable frequency depends on design- and system-specific factors. You should perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Refer to the "Glossary" for definitions of high-speed timing specifications.

Table 1–25 shows the high-speed I/O timing for Stratix III devices.

Table 1–25. True & Emulated LVDS Specifications *(Note 1)*, *(2)* (Part 1 of 3)

Symbol	Conditions	C2			C3, I3			C4, I4			C4L, I4L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency)	Clock boost factor W = 1 to 40 *(3)*	5	—	800	5	—	717	5	—	717	5	—	717	MHz
f_{HSCLK_out} (output clock frequency)	—	5	—	800 *(7)*	5	—	717 *(7)*	5	—	717 *(7)*	5	—	717 *(7)*	MHz
Transmitter														
f_{HSDR} (data rate)	SERDES factor J = 3 to 10 *(8)*	*(4)*	—	1600	*(4)*	—	1250	*(4)*	—	1250	*(4)*	—	1250	Mbps
	SERDES factor J = 2, Uses DDR Register	*(4)*	—	*(4)*	*(4)*	—	*(4)*	*(4)*	—	*(4)*	*(4)*	—	*(4)*	Mbps
	SERDES factor J = 1, Uses SDR Register	*(4)*	—	*(4)*	*(4)*	—	*(4)*	*(4)*	—	*(4)*	*(4)*	—	*(4)*	Mbps
LVDS_E_3R - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	*(4)*	—	1100	*(4)*	—	1100	*(4)*	—	800	*(4)*	—	800	Mbps
LVDS_E_1R - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	*(4)*	—	311	*(4)*	—	200	*(4)*	—	200	*(4)*	—	200	Mbps

Table 1–25. True & Emulated LVDS Specifications *(Note 1)*, *(2)* (Part 3 of 3)

Symbol	Conditions	C2			C3, I3			C4, I4			C4L, I4L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Non DPA Mode														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

Notes to Table 1–25:

(1) When J = 3 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum and maximum specification is dependent on the clock source (PLL and clock pin, for example) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) The $t_{xJitter}$ specification is for true LVDS IO standard only.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing the link timing closure analysis. You should consider the board skew margin, transmitter delay margin as well as the receiver sampling margin to determine the maximum data rate supported.

(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

Table 1–26. Stratix III DPA Lock Time Specifications *(Note 1)*, *(2)*, *(3)* (Part 1 of 2)

Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetitions per 256 data transition *(4)*	Condition *(5)*	Min	Typ	Max
SPI-4	0000000000 1111111111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3×256 data transitions + 2×96 slow clock cycles *(6)*	—	—
Parallel Rapid I/O	00001111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3×256 data transitions + 2×96 slow clock cycles *(6)*	—	—
	10010000	4	64	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3×256 data transitions + 2×96 slow clock cycles *(6)*	—	—

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	N	
产品:	Stratix II	☐
系列:	Stratix II EP2S15	☐
逻辑元件数量:	15600 LE	☐
自适应逻辑模块 - ALM:	6240 ALM	☐
嵌入式内存:	409.5 kbit	☐
输入/输出端数量:	342 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	- 40 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-484	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	780 LAB	
工作电源电流:	250 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	60	
子类别:	Programmable Logic ICs	
总内存:	419328 bit	
商标名:	Stratix II	
零件号别名:	973060	

芯片详细信息

Manufacturer Part Number: EP2S15F484I4	Rohs Code: No	Part Life Cycle Code: Not Recommended	Ihs Manufacturer: INTEL CORP
Package Description: 23 X 23 MM, 1 MM PITCH, FBGA-484	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.26	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 5.117 ns
JESD-30 Code: S-PBGA-B484	JESD-609 Code: e0	Length: 23 mm	Moisture Sensitivity Level: 3
Number of CLBs: 6240	Number of Inputs: 342	Number of Logic Cells: 15600	Number of Outputs: 334
Number of Terminals: 484	Operating Temperature-Max: 100 °C	Operating Temperature-Min: -40 °C	Organization: 6240 CLBS
Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA484,22X22,40	Package Shape: SQUARE
Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 220	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY
Qualification Status: Not Qualified	Seated Height-Max: 3.5 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V
Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS
Temperature Grade: INDUSTRIAL	Terminal Finish: TIN LEAD	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 23 mm	

Table 1–101 specifies EP3SL340 Column Pin delay adders when using the regional clock.

Table 1–101. EP3SL340 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	0.318	0.171	0.255	0.247	0.257	0.244	0.369	0.37	0.253	0.232	0.336	ns
RCLK PLL input adder	2.716	2.739	4.379	4.508	4.926	4.717	5.376	4.508	4.94	4.89	5.434	ns
RCLK output adder	-0.341	-0.107	-0.18	-0.169	-0.171	-0.167	-0.362	-0.03	-0.043	-0.034	-0.287	ns
RCLK PLL output adder	-2.36	-2.128	-3.344	-3.384	-3.571	-3.487	-3.545	-3.246	-3.636	-3.357	-3.544	ns

Table 1–102 specifies EP3SL340 Row Pin delay adders when using the regional clock.

Table 1–102. EP3SL340 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	0.075	0.079	0.133	0.124	0.125	0.124	0.307	0.117	0.116	0.117	0.31	ns
RCLK PLL input adder	0.157	0.151	0.262	0.274	0.306	0.288	0.464	0.268	0.291	0.278	0.46	ns
RCLK output adder	-0.052	-0.066	-0.107	-0.098	-0.127	-0.129	-0.282	-0.082	-0.118	-0.085	-0.285	ns
RCLK PLL output adder	-0.157	-0.139	-0.232	-0.248	-0.272	-0.259	-0.422	-0.252	-0.256	-0.244	-0.444	ns

EP3SE50 I/O Timing Parameters

Table 1–103 through Table 1–106 show the maximum I/O timing parameters for EP3SE50 devices for single-ended I/O standards.

Table 1–103 specifies EP3SE50 column pins input timing parameters for single-ended I/O standards.

Table 1–103. EP3SE50 Column Pins Input Timing Parameters (Part 1 of 4)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.3-V LVTTL	GCLK	t_{su}	-0.911	-0.933	-1.342	-1.477	-1.720	-1.659	-1.949	-1.491	-1.718	-1.662	-1.976	ns
		t_h	1.025	1.062	1.524	1.682	1.947	1.872	2.165	1.705	1.955	1.884	2.193	ns
	GCLK PLL	t_{su}	0.664	0.680	1.158	1.326	1.384	1.294	1.304	1.324	1.397	1.302	1.361	ns
		t_h	-0.421	-0.422	-0.773	-0.891	-0.897	-0.838	-0.836	-0.880	-0.901	-0.838	-0.890	ns
3.3-V LVCMOS	GCLK	t_{su}	-0.911	-0.933	-1.342	-1.477	-1.720	-1.659	-1.949	-1.491	-1.718	-1.662	-1.976	ns
		t_h	1.025	1.062	1.524	1.682	1.947	1.872	2.165	1.705	1.955	1.884	2.193	ns
	GCLK PLL	t_{su}	0.664	0.680	1.158	1.326	1.384	1.294	1.304	1.324	1.397	1.302	1.361	ns
		t_h	-0.421	-0.422	-0.773	-0.891	-0.897	-0.838	-0.836	-0.880	-0.901	-0.838	-0.890	ns