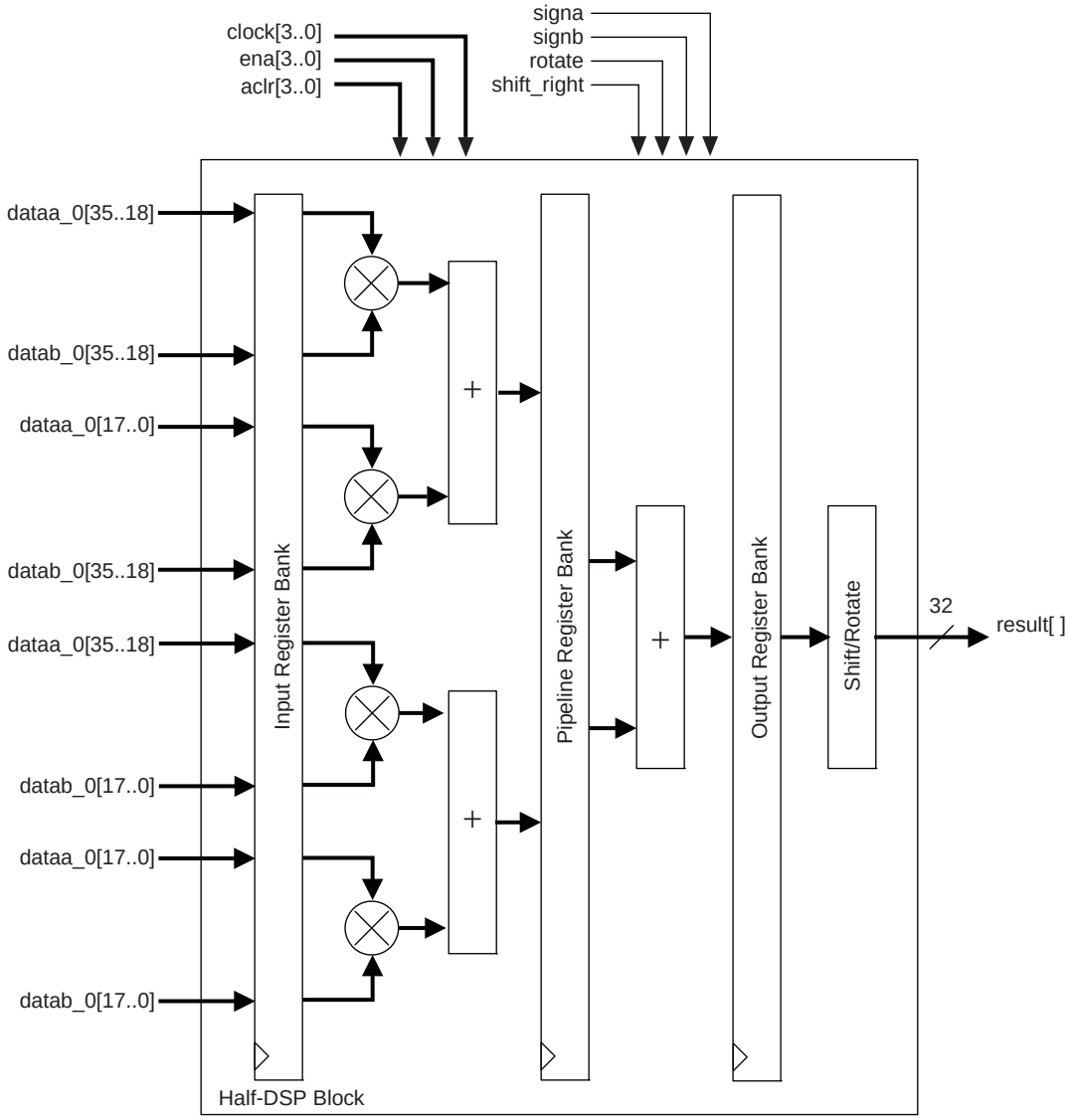
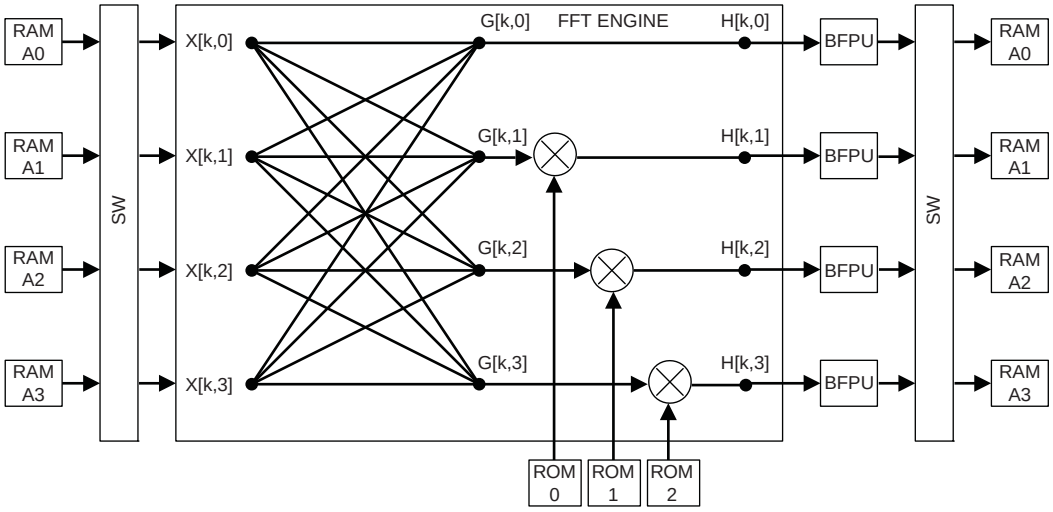
Figure 5–20. Shift Operation Mode for Half-DSP Block



In Figure 5–25, a radix-4 butterfly is shown. Each butterfly requires three complex multipliers. This can be implemented in Stratix III using three half-DSP blocks assuming that the data and twiddle wordlengths are 18 bits or fewer.

Figure 5–25. Radix-4 Butterfly



Software Support

Altera provides two distinct methods for implementing various modes of the DSP block in a design: instantiation and inference. Both methods use the following Quartus II megafunctions:

- LPM_MULT
- ALTMULT_ADD
- ALTMULT_ACCUM
- ALTFP_MULT

You can instantiate the megafunctions in the Quartus II software to use the DSP block. Alternatively, with inference, you can create an HDL design and synthesize it using a third-party synthesis tool (such as LeonardoSpectrum, Synplify, or Quartus II Native Synthesis) that infers the appropriate megafunction by recognizing multipliers, multiplier adders, multiplier accumulators, and shift functions. Using either method, the Quartus II software maps the functionality to the DSP blocks during compilation.

For instructions about using the megafunctions and the *MegaWizard Plug-In Manager*, refer to the *Quartus II Software Help*.

For more information, refer to the *Synthesis* section in volume 1 of the *Quartus II Development Software Handbook*.

EP3SL110F780I3LN	50	BGA	20+	ALTERA
EP3SL110F780I3N	120	BGA	20+	ALTERA
EP3SL110F780I4LN	25	BGA	20+	ALTERA
EP3SL110F780I4N	6	BGA	20+	Intel/Altera
EP3SL110F780I4N	280	BGA	20+	ALTERA
EP3SL150F1152C4N	5	BGA	20+	Intel/Altera
EP3SL150F1152C4N	163	FBGA900	20+	ALTERA
EP3SL150F1152C4N	1000	BGA	20+	ALTERA
EP3SL150F1152I3N	300	BGA	20+	ALTERA
EP3SL150F1152I4N	500	BGA	20+	ALTERA
EP3SL150F780C2N	152	BGA	20+	ALTERA
EP3SL150F780I3N	1010	SOP	20+	ALTERA
EP3SL200F1152I3N	228	BGA	20+	ALTERA
EP3SL200F1152I4N	105	FBGA676	20+	ALTERA
EP3SL200F1517C3N	70	BGA	20+	ALTERA
EP3SL200H28I3N	50	BGA	20+	XILINX
EP3SL200H780C4N	285	FBGA780	20+	ALTERA
EP3SL260F1517C3N	68	BGA	20+	ALTERA
EP3SL340F1517C2N	200	BGA	20+	ALTERA
EP3SL340F1517C3N	100	BGA	20+	ALTERA
EP3SL340F1517C4N	105	BGA	20+	ALTERA
EP3SL340F1517I3N	3	BGA	20+	Intel/Altera
EP3SL340F1517I3N	371	FCBGA1136	20+	ALTERA
EP3SL340F1517I4N	321	BGA	20+	ALTERA
EP3SL340H1152I3N	136	BGA	20+	Intel/Altera
EP3SL340H1152I4N	256	BGA	20+	ALTERA
EP3SL50F780C3N	140	BGA	20+	Intel/Altera
EP3SL50F780C4N	133	BGA	20+	ALTERA
EP4S100G5F45I1N	200	BGA	20+	Intel/Altera
EP4S100G5F45I1N	50	BGA	20+	ALTERA
EP4S40G2F40I2N	120	BGA	20+	XILINX
EP4S40G5H40I2N	25	BGA	20+	ALTERA
EP4S40G5H40I2N	40	BGA	20+	Intel/Altera
EP4S40G5H40I2NAD	60	BGA	20+	ALTERA
EP4S40G5H40I4N	220	FBGA1158	20+	ALTERA
EP4SE230F29C4N	8	BGA	20+	ALTERA
EP4SE230F29I3N	60	BGA	20+	ALTERA

EP4S40G5H40I2NAD	60	BGA	20+	ALTERA
EP4S40G5H40I4N	220	FBGA1158	20+	ALTERA
EP4SE230F29C4N	8	BGA	20+	ALTERA
EP4SE230F29I3N	60	BGA	20+	ALTERA
EP4SE230F29I4N	68	FCBGA900	20+	ALTERA
EP4SE230F29IN	500	BGA	20+	ALTERA
EP4SE230F35I4N	200	BGA	20+	ALTERA
EP4SE360F35I3N	100	BGA	20+	ALTERA
EP4SE360F35I4N	364	FCBGA1136	20+	ALTERA
EP4SE360F35I4N	1178	LFCSP	20+	ALTERA
EP4SE530H35C4N	22000	SOP8	20+	ALTERA
EP4SE530H35I3N	73	BGA	20+	ALTERA
EP4SE530H35I4N	385	FCBGA1156	20+	ALTERA
EP4SGX110HF35C2N	35	BGA	20+	ALTERA
EP4SGX110HF35C4N	60	BGA	20+	ALTERA
EP4SGX110HF35I3N	50	BGA	20+	ALTERA
EP4SGX180DF29I3N	130	BGA	20+	ALTERA
EP4SGX180DF29I4N	260	FBGA1152	20+	ALTERA
EP4SGX180FF35C3N	176	FCBGA1156	20+	ALTERA
EP4SGX180FF35C4N	156	BGA484	20+	ALTERA
EP4SGX180FF35I3N	21	BGA	20+	ALTERA
EP4SGX180FF35I4N	178	BGA	20+	ALTERA
EP4SGX180KF20C2N	12	BGA	20+	ALTERA
EP4SGX180KF40C2N	5500	1808SMD	20+	ALTERA
EP4SGX180KF40C4N	48	BGA	20+	ALTERA
EP4SGX180KF40I3N	62	BGA	20+	Intel/Altera
EP4SGX180KF40I4N	3197	BGA	20+	ALTERA
EP4SGX230FF35C3N	155	FCBGA1136	20+	ALTERA
EP4SGX230FF35C3N	50	BGA	20+	ALTERA
EP4SGX230FF35C4N	185	BGA	20+	ALTERA
EP4SGX230FF35I3N	120	BGA	20+	ALTERA
EP4SGX230FF35I3N	101	BGA	20+	ALTERA
EP4SGX230FF35I4N	500	BGA	20+	ALTERA
EP4SGX230FF35I4N	100	BGA	20+	ALTERA
EP4SGX230HF35C2N	152	BGA	20+	ALTERA
EP4SGX230HF35I3N	160	BGA	20+	ALTERA
EP4SGX230HF35I4N	72	BGA	20+	ALTERA

Table 6–6 lists the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 4. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–6. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 4)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK6	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK7	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK8	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK9	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
RCLK10	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK11	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK12	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK13	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK14	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK15	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK16	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK17	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK18	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK19	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK20	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK21	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—

Table 6–7 lists the dedicated clock input pin connectivity to Stratix III device PLLs.

Table 6–7. Stratix III Device PLLs and PLL Clock Pin Drivers (Part 1 of 2) *(Note 1)*

Dedicated Clock Input Pin (CLKp/n pins)	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
CLK0	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK1	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK2	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK3	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK4	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK5	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK6	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK7	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK8	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK9	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK10	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK11	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK12	—	—	—	—	—	—	—	—	—	—	✓	✓