Configuration Watchdog Timer Register

The configuration watchdog timer (CWDT) register stores the value of the number of clock cycles that the FPGA will wait before the watchdog time-out (in which SYNCWORD is not received). The default is 64k clock cycles. The minimum value is `16h'0201`.

Table 5-39: **CWDT Register**

Bits	Value
[15:0]	`16h'ffff`

HC_OPT_REG Register

The HC_OPT_REG register can only be reset to default by por_b.

Table 5-40: **HC_OPT_REG Description**

Name	Bits	Description	Default
INIT_SKIP	6	`0`: Do not skip initialization. `1`: Skip initialization.	`0`
RESERVED	5:0	Reserved.	`011111`

GENERAL Registers 1, 2, 3, 4, and 5

GENERAL1 and GENERAL2 registers are used to store loadable multiple configuration addresses for SPI and BPI.

GENERAL3 and GENERAL4 registers have a similar function as GENERAL1 and GENERAL2, except that GENERAL3 and GENERAL4 store the golden bitstream address instead of the MultiBoot address.

The GENERAL5 register is a 16-bit register that allows users to store and access any extra information desired for the fail-safe scheme. These register contents are untouched during a soft reboot.

These registers are set by the bitstream. BitGen can be instructed not to write to these registers using the -g next_config_register_write:Disable command. This allows the ability to store user data in the FPGA between re-configuration attempts.

Table 5-41: **General Registers**

Name	Bits	Description
GENERAL1	[15:0]	The lower half of the multiple boot address.
GENERAL2	[15:0]	15:8 – SPI opcode. 7:0 – Higher half of the boot address.
GENERAL3	[15:0]	The lower half of the *golden* bitstream address.
GENERAL4	[15:0]	15:8 – SPI opcode. 7:0 – Higher half of the golden boot address.
GENERAL5	[15:0]	The user-defined scratchpad register.

If the second configuration needs a previously unknown SPI vendor command, the new vendor command has already been loaded in GENERAL2 from the bitstream by this point.

Configuration Register Read Procedure (SelectMAP)

The simplest read operation targets a configuration register such as the COR0 or STAT register. Any configuration register with read access can be read through the SelectMAP interface, although not all registers offer read access. The procedure for reading the STAT register through the SelectMAP interface follows:

1. Write a dummy word and a synchronization word to the device followed by at least one no operation command (NOOP).
2. Write the *read STAT register* packet header to the device.
3. Write four NOOPs to the device to flush the packet buffer.
4. Read one word from the SelectMAP interface; this is the Status register value.
5. Write the DESYNC command to the device.
6. Write two NOOPs to the device to flush the packet buffer.

Table 6-1: **Status Register Readback Command Sequence (16-Bit SelectMAP)**

Step	SelectMAP Port Direction	Configuration Data [15:0]	Explanation
1	Write	FFFF	Dummy Word
2	Write	FFFF	Dummy Word
3	Write	AA99	Sync Word
4	Write	5566	Sync Word
5	Write	2000	NOOP
6	Write	2901	Write Type1 packet header to read STAT register
7	Write	2000	NOOP
8	Write	2000	NOOP
9	Write	2000	NOOP
10	Write	2000	NOOP
11	Read	SSSS	Read one word from the STAT register to the configuration interface
12	Write	30A1	Type 1 Write 1 Word to CMD
13	Write	000D	DESYNC Command
14	Write	2000	NOOP
15	Write	2000	NOOP

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Virtex-II Pro	☐
系列:	XC2VP30	☐
逻辑元件数量:	30816 LE	☐
自适应逻辑模块 - ALM:	13696 ALM	☐
嵌入式内存:	2.39 Mbit	☐
输入/输出端数量:	664 I/O	☐
工作电源电压:	1.5 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-1152	☐
数据速率:	4.25 Gb/s	
商标:	Xilinx	
分布式RAM:	428 kbit	
内嵌式块RAM - EBR:	2448 kbit	
最大工作频率:	300 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	3424 LAB	
收发器数量:	8 Transceiver	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	24	
子类别:	Programmable Logic ICs	
商标名:	Virtex	

After the configuration logic receives the IPROG command, the FPGA resets everything except the dedicated reconfiguration logic, and the INIT_B and DONE pins go Low. After the FPGA clears all configuration memory, INIT_B goes High again. Then the value in GENERAL1,2 is used for the bitstream starting address.

IPROG does not reset the strike count. MultiBoot applications that use IPROG through ICAP_SPARTAN6 should pulse PROGRAM_B or implement a power cycle after a configuration error that increments the strike count. Otherwise, verify that external memory is properly updated to avoid configuration errors that would increment the strike count.

Status Register for Fallback and IPROG Reconfiguration

Spartan-6 devices contain a BOOTSTS that stores configuration history. At EOS or an error condition, Status_0 is updated with the current status. If fallback or MultiBoot occurs, Status_1 is updated at EOS or an error condition. The Valid_0 bit indicates if the rest of Status_0 is valid or not. The BOOTSTS register is written either at an End Of Startup (EOS) event or a fallback event. The EOS event happens after the first configuration attempt. A successful MultiBoot operation via the IPROG command does not result in the BOOTSTS register being updated. See Boot History Status Register (BOOTSTS), page 110.

Table 7-2 through Table 7-4 show the BOOTSTS values in some common situations.

Table 7-2: **Status after First Bitstream Configuration without Error**

	CRC_ERROR	ID_ERROR	WTO_ERROR	IPROG	FALLBACK	VALID
Status_1	0	0	0	0	0	0
Status_0	0	0	0	0	0	1

Table 7-3: **First Configuration followed by IPROG**

	CRC_ERROR	ID_ERROR	WTO_ERROR	IPROG	FALLBACK	VALID
Status_1	0	0	0	0	0	1
Status_0	0	0	0	1	0	1

Table 7-4: **IPROG Embedded in First Bitstream, Second Bitstream CRC Error, and Fallback Successfully**

	CRC_ERROR(1)	ID_ERROR	WTO_ERROR	IPROG	FALLBACK	VALID
Status_1(2)	0	0	0	1	1	1
Status_0(3)	1	0	0	1	0	1

Notes:

1. CRC_Error only registers CRC errors detected during initial configuration. CRC_Error is not updated if CRC errors are found from the Readback CRC (POST_CRC) function.
2. Status_1 shows a fallback bitstream was loaded successfully. The IPROG bit was also set in this case, because the fallback bitstream contains an IPROG command. Although the IPROG command is ignored during fallback, the status still records this occurrence.
3. Status_0 shows IPROG was attempted, and a CRC_ERROR was detected for that bitstream.

XC3195APQ160CKG	2001+	QFP	2315
XC3195A-PQ160AKJ	2001+	QFP	2315
XC3195APQ160AKJ	2001+	QFP	2315
XC3195APQ160-5C	2001+	QFP	2315
XC3195A-PQ160-4C	2001+	QFP	2315
XC3195APQ160-3C	2001+	QFP	2315
XC3195APQ160-2C	2001+	QFP	2315
XC3195APQ160-1C	2001+	QFP	2315
XC3195A-PQ160	2001+	QFP	2315
XC3195APQ160	2001+	QFP	2315
XC3195APQ	2001+	QFP	2315
XC3195APP175CKG	2001+	PGA	2315
XC3195APP175C-3	2001+	QFP	2315
XC3195A-PP175C	2001+	PGA	2315
XC3195APP175-3C	2001+	PGA	2315
XC3195APG175CKG	2001+	PGA	2315
XC3195A-PC84AKJ	2001+	PLCC-84	2315
XC3195APC84AKJ	2001+	PLCC84	2315
XC3195APC84-5C	2001+	PLCC	2315
XC3195A-9PC84C	2001+	PLCC84	2315
XC3195A-6PQ160	2001+	QFP	2315
XC3195A-6PC84C	2001+	PLCC	2315
XC3195A-5PQ208I	2001+	QFP	2315
XC3195A-5PQ208C	2001+	TQFP	2315
XC3195A-5PQ160I	2001+	BGA	2315
XC3195A-5PQ160C	2001+	QFP-160	2315
XC3195A-5PQ160	2001+	PLCC	2315
XC3195A-5PG175M	2001+	PGA	2315
XC3195A-5PG175I	2001+	BGA	2315
XC3195A-5PG175C	2001+	PGA	2315
XC3195A-5PG175B	2001+	PGA	2315
XC3195A-5PC84I	2001+	PLCC84	2315
XC3195A-5PC84C	2001+	PLCC84	2315
XC3195A-5PC84	2001+	PLCC84	2315
XC3195A-5	2001+	QFP	2315
XC3195A-4PQG160I	2001+	QFP160	2315
XC3195A-4PQG160C	2001+	QFP160	2315
XC3195A-4PQ208I	2001+	QFP	2315
XC3195A-4PQ208C	2001+	BGAQFP	2315
XC3195A-4PQ160I	2001+	QFP160	2315
XC3195A-4PQ160C	2001+	QFP160	2315